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# A-826PG

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## *Hardware User's Manual*

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# 1. Introduction

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## 1.1 General Description

The A-826PG is a 16 bit high performance, multi-function analog, digital I/O board for the PC AT compatible computer. A software programmable gain amplifier has gain of 1, 2, 4, 8. The A-826PG offers 16 single-ended or 8 differential analog inputs. The maximum sample rate of the A/D converter is about 100 k sample/sec. There are two 12-bits DAC with voltage outputs, 16 channels of TTL-compatible digital input, 16 channels of TTL-compatible digital output and one 16-bit counter/timer channel for timing input and output.

Using ASC-TI486/33 M CPU board of ICP as testing platform, the conversion speed of A-826PG is given below:

- **Polling mode : about 100 k sample/sec.**
- **Interrupt mode : about 60 k sample/sec.**
- **DMA mode : about 100 k sample/sec.**

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## 1.2 Features

- 16 Bit high resolution & high speed
- The maximum sample rate of the A/D converter is about 100 k sample/sec.
- 16 single-ended or 8 differential analog input signals
- Software selectable input ranges
- A/D trigger mode : software trigger , pacer trigger, external trigger , event trigger
- Programmable gain of 1,2,4 or 8
- 2 channel of 12-bit D/A voltage output
- 16 digital input /16 digital output (TTL compatible)
- Interrupt handling
- Bipolar operation
- 1 channel general purpose programmable 16 bits timer/counter

- PC AT compatible ISA bus

## 1.3 Specifications

| Model Name              | A-826PG   |
|-------------------------|---|
| <b>Analog Input</b>     |   |
| Channels                | 16 single-ended / 8 differential                |
| A/D Converter           | 16-bit, 8 $\mu$ s conversion time               |
| Sampling Rate           | 100 kS/s. max.                                  |
| Over voltage Protection | Continuous +/-35 Vp-p                           |
| Input Impedance         | 10 M $\Omega$ /6pF                              |
| Trigger Modes           | Software, Pacer, External, Event                |
| Data Transfer           | Polling, Interrupt, DMA                         |
| Accuracy                | 0.01 % of FSR $\pm$ 1 LSB @ 25 °C, $\pm$ 10 V   |
| Zero Drift              | 15 ppm/°C of FSR                                |
| <b>Analog Output</b>    |   |
| Channels                | 2 independent                                   |
| Resolution              | 12-bit  |
| Accuracy                | 0.01% of FSR $\pm$ 1 LSB @ 25 °C, $\pm$ 10 V    |
| Output Range            | 0 ~ 5 V, 0 ~ 10 V or 0 ~ Ext Ref                |
| External Reference      | +10 V or -10 V (max.)                           |
| Output Driving          | +/- 5 mA  |
| Slew Rate               | 0.6 V/ $\mu$ s                                  |
| Output Impedance        | 0.1 $\Omega$ max.                               |
| Operating Mode          | Software  |
| <b>Digital Input</b>    |   |
| Channels                | 16  |
| Compatibility           | 5 V/TTL   |
| Input Voltage           | Logic 0: 0.8 V max.<br>Logic 1: 2.0 V min.      |
| Response Speed          | 1.0 MHz (Typical)                               |
| <b>Digital Output</b>   |   |
| Channels                | 16  |
| Compatibility           | 5 V/TTL   |
| Output Voltage          | Logic 0: 0.4 V (max.)<br>Logic 1: 2.4 V (min.)  |
| Output Capability       | Sink: 0.8 mA @ 0.8 V<br>Source: -2.4 mA @ 2.0 V |
| Response Speed          | 1.0 MHz (Typical)                               |
| <b>Timer/Counter</b>    |   |
| Channels                | 3 independent                                   |
| Resolution              | 16-bit  |
| Compatibility           | 5 V/TTL   |
| Input Frequency         | 10 MHz max.                                     |
| Reference Clock         | Internal: 2 MHz                                 |
| <b>General</b>          |   |
| Bus Type                | ISA   |
| I/O Connector           | Female DB37 x 1<br>20-pin box header x 2        |
| Dimensions (L x W x D)  | 175 mm x 122 mm x 22 mm                         |
| Power Consumption       | 950 mA @ +5 V                                   |
| Operating Temperature   | 0 ~ 60 °C                                       |
| Storage Temperature     | -20 ~ 70 °C                                     |
| Humidity                | 5 ~ 85% RH, non-condensing                      |

- 
- Analog Input Range (software programmable)

| Model         | A-826PG  |       |         |          |
|---------------|----------|-------|---------|----------|
| Gain          | 1        | 2     | 4       | 8        |
| Bipolar (V)   | +/- 10   | +/- 5 | +/- 2.5 | +/- 1.25 |
| Sampling Rate | 100 kS/s |       |         |          |

---

### 1.3.1 Direct Memory Access Channel (DMA)

- Level : CH1 or CH3, jumper selectable
- Enable : via DMA bit of control register
- Termination : by interrupt on T/C
- Transfer rate : 100 k conversions/sec.(DOS Software manual, sec. 4.11)

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## 1.4 Applications

- Signal analysis
- FFT & frequency analysis
- Transient analysis
- Production test
- Process control
- Vibration analysis
- Energy management
- Industrial and lab. measurement and control

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## 1.5 Product Check List

The package includes the following items:

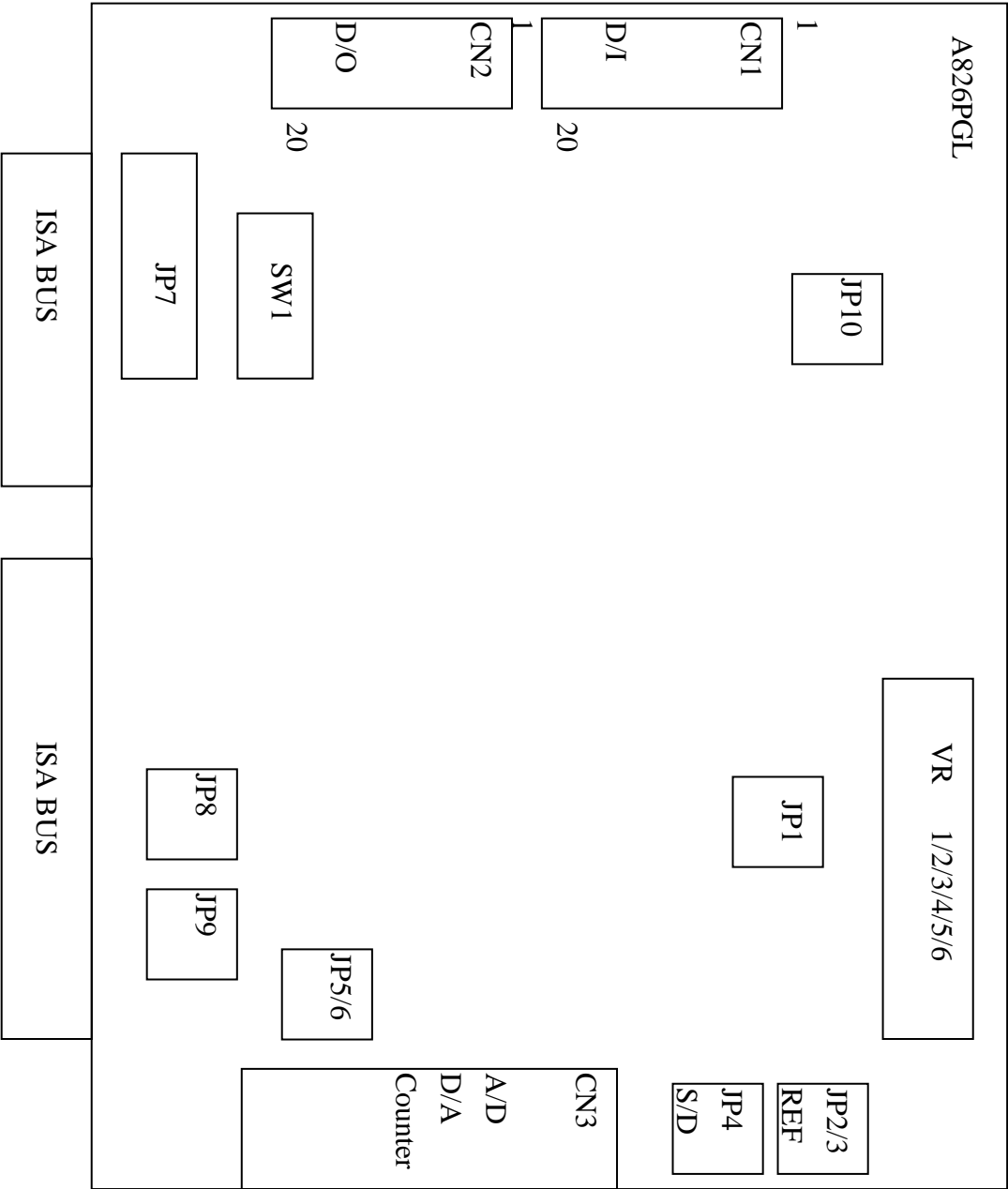
- One piece of A-826PG multifunction card
- One company floppy diskette or CD
- One Quick Start Guide

### **Attention !**

If any of these items are missing or damaged, contact the dealer who provided you with this product. Save the shipping materials and carton in case you want to ship or store the product in the future.

# 2. Hardware Configuration

## 2.1 Board Layout





# 2.2 I/O Base Address Setting

The A-826PG occupies 16 consecutive locations in I/O address space. The base address is set by DIP switch SW1. The default address is 0x220.



## For Example

### How to select 2 2 0 (Hex)

OFF → 1  
 ON → 0

|     |    |    |    |     |    |   |
|-----|----|----|----|-----|----|---|
| 2   |    | 2  |    |     |    | 0 |
| OFF | ON | ON | ON | OFF | ON |   |
| 1   | 0  | 0  | 0  | 1   | 0  |   |
| A9  | A8 | A7 | A6 | A5  | A4 |   |

→

The detail SW1 base addresses setting. Please refer to **2.2.1 Base Address Table**.

## 2.2.1 Base Address Table:

| IO Address        | 1<br>A9    | 2<br>A8   | 3<br>A7   | 4<br>A6   | 5<br>A5    | 6<br>A4   |
|-------------------|------------|-----------|-----------|-----------|------------|-----------|
| 200-20F           | OFF        | ON        | ON        | ON        | ON         | ON        |
| 210-21F           | OFF        | ON        | ON        | ON        | ON         | OFF       |
| <b>220-22F(*)</b> | <b>OFF</b> | <b>ON</b> | <b>ON</b> | <b>ON</b> | <b>OFF</b> | <b>ON</b> |
| 230-23F           | OFF        | ON        | ON        | ON        | OFF        | OFF       |
| 240-24F           | OFF        | ON        | ON        | OFF       | ON         | ON        |
| 250-25F           | OFF        | ON        | ON        | OFF       | ON         | OFF       |
| 260-26F           | OFF        | ON        | ON        | OFF       | OFF        | ON        |
| 270-27F           | OFF        | ON        | ON        | OFF       | OFF        | OFF       |
| 280-28F           | OFF        | ON        | OFF       | ON        | ON         | ON        |
| 290-29F           | OFF        | ON        | OFF       | ON        | ON         | OFF       |
| 2A0-2AF           | OFF        | ON        | OFF       | ON        | OFF        | ON        |
| 2B0-2BF           | OFF        | ON        | OFF       | ON        | OFF        | OFF       |
| 2C0-2CF           | OFF        | ON        | OFF       | OFF       | ON         | ON        |
| 2D0-2DF           | OFF        | ON        | OFF       | OFF       | ON         | OFF       |
| 2E0-2EF           | OFF        | ON        | OFF       | OFF       | OFF        | ON        |
| 2F0-2FF           | OFF        | ON        | OFF       | OFF       | OFF        | OFF       |
| 300-30F           | OFF        | OFF       | ON        | ON        | ON         | ON        |
| 310-31F           | OFF        | OFF       | ON        | ON        | ON         | OFF       |
| 320-32F           | OFF        | OFF       | ON        | ON        | OFF        | ON        |
| 330-33F           | OFF        | OFF       | ON        | ON        | OFF        | OFF       |
| 340-34F           | OFF        | OFF       | ON        | OFF       | ON         | ON        |
| 350-35F           | OFF        | OFF       | ON        | OFF       | ON         | OFF       |
| 360-36F           | OFF        | OFF       | ON        | OFF       | OFF        | ON        |
| 370-37F           | OFF        | OFF       | ON        | OFF       | OFF        | OFF       |
| 380-38F           | OFF        | OFF       | OFF       | ON        | ON         | ON        |
| 390-39F           | OFF        | OFF       | OFF       | ON        | ON         | OFF       |
| 3A0-3AF           | OFF        | OFF       | OFF       | ON        | OFF        | ON        |
| 3B0-3BF           | OFF        | OFF       | OFF       | ON        | OFF        | OFF       |
| 3C0-3CF           | OFF        | OFF       | OFF       | OFF       | ON         | ON        |
| 3D0-3DF           | OFF        | OFF       | OFF       | OFF       | ON         | OFF       |
| 3E0-3EF           | OFF        | OFF       | OFF       | OFF       | OFF        | ON        |
| 3F0-3FF           | OFF        | OFF       | OFF       | OFF       | OFF        | OFF       |

(\*) : default base address is 0x220

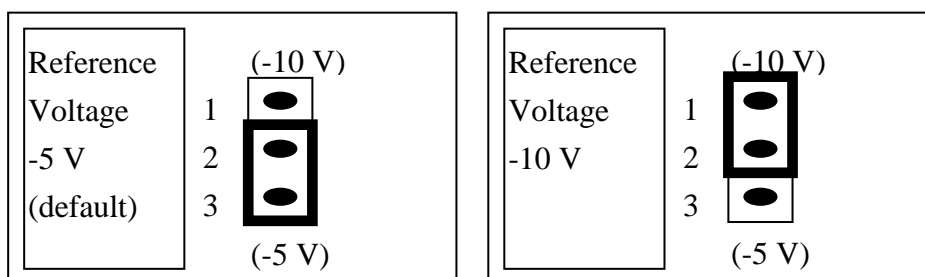
The PC I/O port mapping is given below.

| ADDRESS | Device                   | ADDRESS | DEVICE               |
|---------|--------------------------|---------|----------------------|
| 000-1FF | PC reserved              | 320-32F | XT Hard Disk         |
| 200-20F | Game/control             | 378-37F | Parallel Printer     |
| 210-21F | XT Expansion Unit        | 380-38F | SDLC                 |
| 238-23F | Bus Mouse/Alt. Bus Mouse | 3A0-3AF | SDLC                 |
| 278-27F | Parallel Printer         | 3B0-3BF | MDA/Parallel Printer |
| 2B0-2DF | EGA                      | 3C0-3CF | EGA                  |
| 2E0-2E7 | AT GPIB                  | 3D0-3DF | CGA                  |
| 2E8-2EF | Serial Port              | 3E8-3EF | Serial Port          |
| 2F8-2FF | Serial Port              | 3F0-3F7 | Floppy Disk          |
| 300-31F | Prototype Card           | 3F8-3FF | Serial Port          |

## 2.3 Jumper Setting

### 2.3.1 JP1 : D/A Internal Reference Voltage

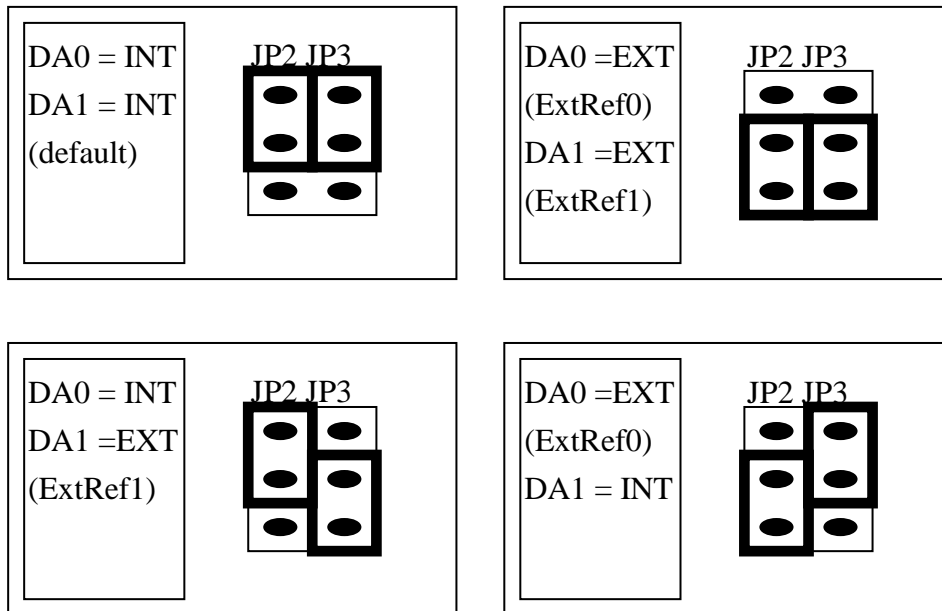
#### Selection



Select (-5 V) : Voltage output range = 0 ~ +5 V<sub>DC</sub> for both D/A channels  
 Select (-10 V): Voltage output range = 0 ~ +10 V<sub>DC</sub> for both D/A channels

**Note that JP1 is valid only if JP2 /JP3 select D/A internal reference voltage.**

## 2.3.2 JP2/JP3 : D/A Int/Ext Ref Voltage Selection



If JP2 or JP3 jumper is configured in **INT** position, the JP1 jumper must be configured to provide -5 V or -10 V internal reference voltage for D/A (see [Section 2.3.1](#)).

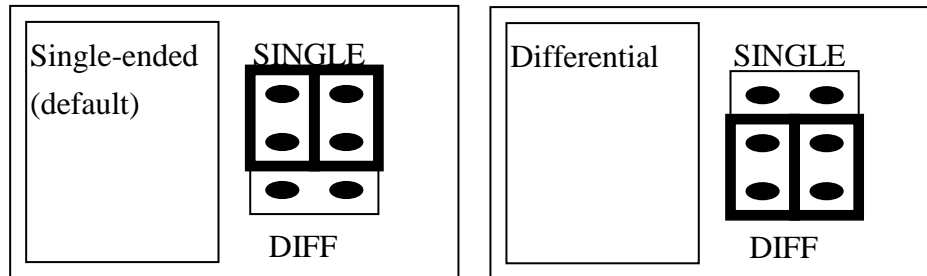
If JP2 or JP3 jumper is configured in **EXT** position, the respective **ExtRef0 (CN3 pin 31)** and **ExtRef1 (CN3 pin 12)** must be used to provide the **external reference voltage** for DA0 and DA1.

The provided **external reference voltage range is -10 V<sub>DC</sub> to +10 V<sub>DC</sub>**, and the DA voltage output range is as follows:

| Channel                        | Pin Assignments  | External Reference Voltage (V <sub>DC</sub> ) | Voltage Output Range (V <sub>DC</sub> ) |
|--------------------------------|--|---|---|
| DA0 (ExtRef0)<br>DA1 (ExtRef1) | CN3, Pin31<br>CN3, Pin12<br>(see <a href="#">Chapter 3</a> ) | Ext Ref (User-defined)                        | 0 ~ Ext Ref                             |
|                                |  | + 10 V <sub>DC</sub> (Max.)                   | 0 ~ -10 V <sub>DC</sub>                 |
|                                |  | -10 V <sub>DC</sub> (Max.)                    | 0 ~ +10 V <sub>DC</sub>                 |

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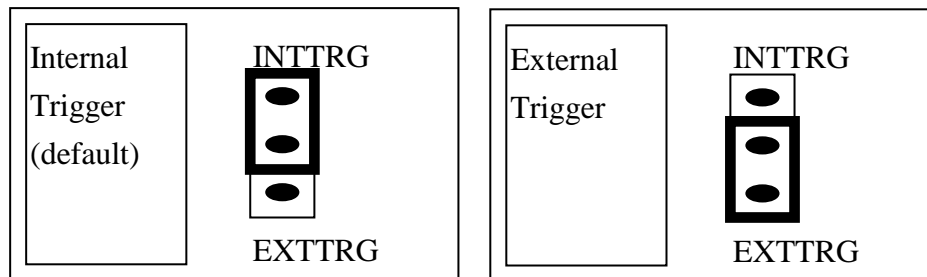
### 2.3.3 JP4 : Single-ended/Differential Selection



The A-826PG offers 16 single-ended or 8 differential analog input signals. The JP4 selects single-ended/differential. The user cannot select single-ended and differential simultaneously.

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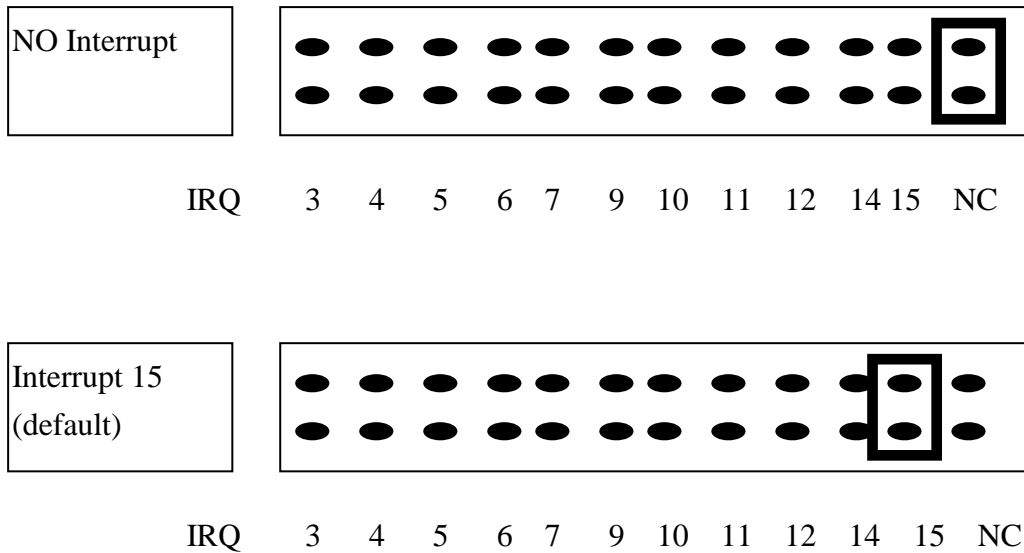
### 2.3.4 JP5 : A/D Trigger Source Selection



The A-826PG supports two trigger type, **internal trigger** and **external trigger**. The external trigger signal comes from **ExtTrg, CN3 pin 17**. There are two types of internal trigger, **software trigger** and **pacer trigger**.

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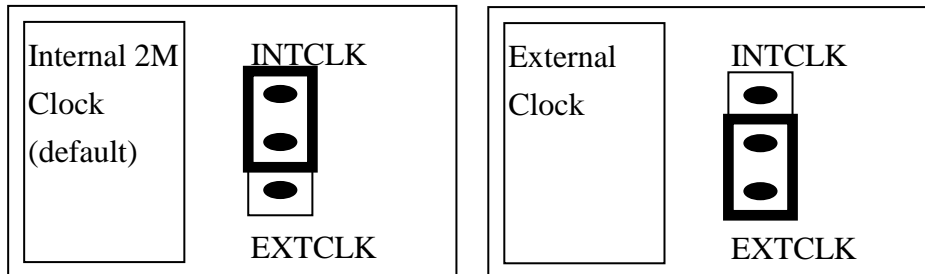
### 2.3.5 JP7 : Interrupt Level Selection



The interrupt channel **can not be shared.** The A826 software driver can support 8 different boards in one system but only **2 of these cards** can use interrupt transfer function.

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## 2.3.6 JP6 : User Timer/Counter Clock Input Selection



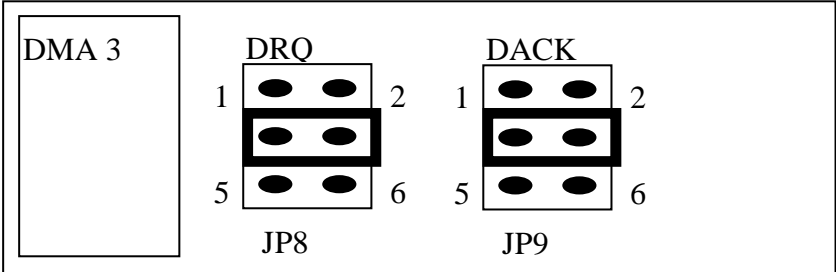
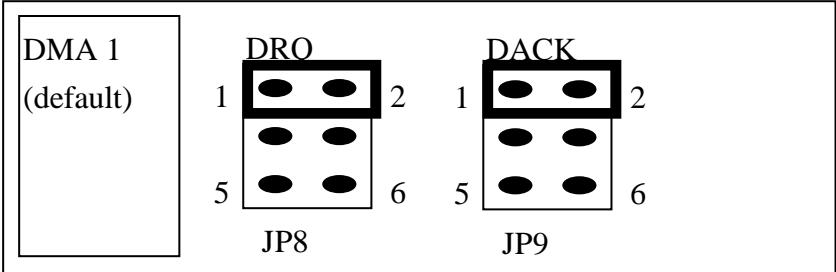
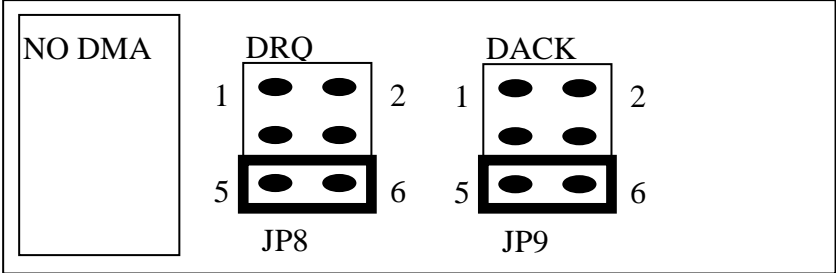
The A-826PG has 3 independent 16 bits timer/counter. The cascaded counter1 and counter2 are used as **pacemaker timer**. Counter0 can be use as a user programmable timer/counter. The user programmable timer/counter can select **2 M internal clock** or **external clock ExtCLK, CN3 pin 37**. The block diagram is given in section 2.6. The clock source must be very **stable**. It is recommended to use internal 2 M clock.

The A-826PG software driver uses counter0 as a machine independent timer. Users can use **A826\_Delay()** subroutine to program counter 0 as a machine independent timer. Detailed information is given in section 2.6.

**NOTE : if using A826\_Delay(), the JP6 must select internal 2 M clock.**

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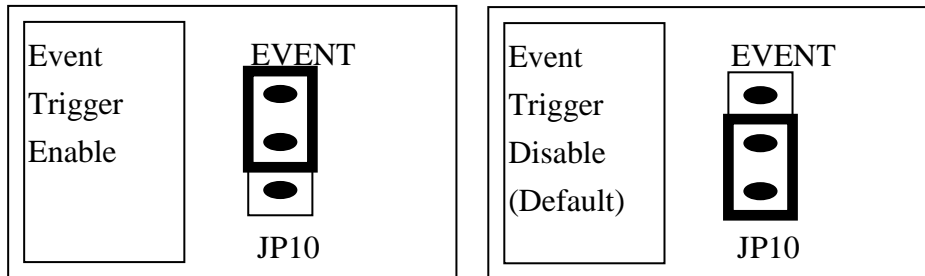
### 2.3.7 JP8 : DMA DACK Selection, JP9 : DMA DRQ Selection



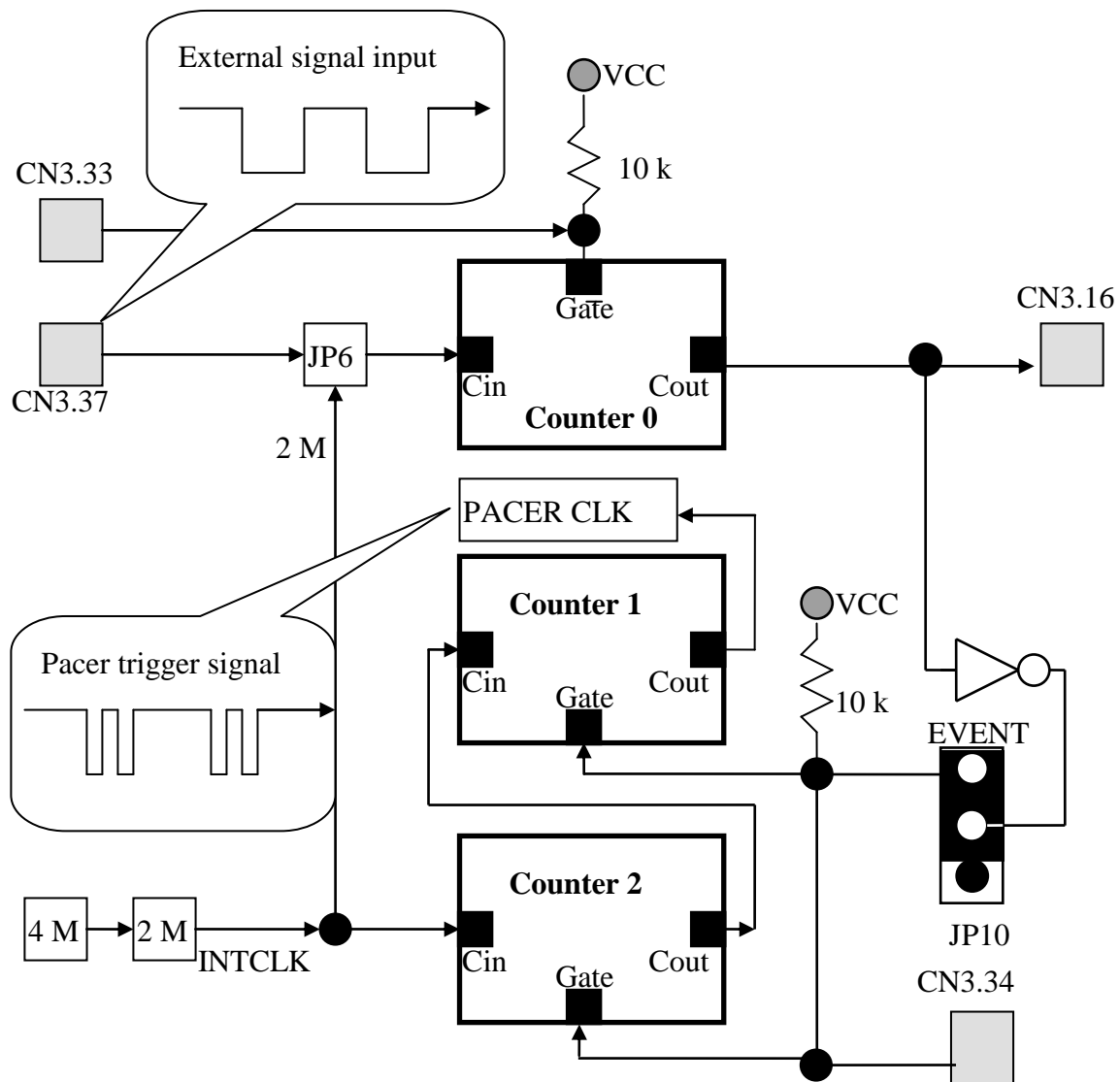
**The DMA channel cannot share.** The A826 software driver can support 8 different boards in one PC based system, but only **two of these boards** can use DMA transfer function.



## 2.3.8 JP10 : Event Trigger Selection



Both of the machine independent timer and the event trigger controller use timer/counter 0. Only one of these two functions can be implemented. **So the user can not use both function at the same time.**



---

## 2.3.9 I/O Register Address

The A-826PG occupies 16 consecutive PC I/O addresses. The following table lists the registers and their locations.

| <b>Address</b> | <b>Read</b>          | <b>Write</b>                 |
|----------------|----------------------|------------------------------|
| Base+0         | 8254 Counter 0       | 8254 Counter 0               |
| Base+1         | 8254 Counter 1       | 8254 Counter 1               |
| Base+2         | 8254 Counter 2       | 8254 Counter 2               |
| Base+3         | Reserved             | 8254 Counter Control         |
| Base+4         | A/D Low Byte         | D/A Channel 0 Low Byte       |
| Base+5         | A/D High Byte        | D/A Channel 0 High Byte      |
| Base+6         | DI Low Byte          | D/A Channel 1 Low Byte       |
| Base+7         | DI High Byte         | D/A Channel 1 High Byte      |
| Base+8         | A/D Conversion Ready | A/D Clear Interrupt Request  |
| Base+9         | Reserved             | A/D Gain Control             |
| Base+A         | Reserved             | A/D Multiplexer Control      |
| Base+B         | Reserved             | A/D Mode Control             |
| Base+C         | Reserved             | A/D Software Trigger Control |
| Base+D         | Reserved             | DO Low Byte                  |
| Base+E         | Reserved             | DO High Byte                 |

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## 2.3.10 8254 Counter

The 8254 Programmable timer/counter has 4 registers from Base+0 through Base+3. For detailed programming information about the 8254, please refer to Intel's "Microsystem Components Handbook".

| Address | Read           | Write                |
|---------|----------------|----------------------|
| Base+0  | 8254 Counter 0 | 8254 Counter 0       |
| Base+1  | 8254 Counter 1 | 8254 Counter 1       |
| Base+2  | 8254 Counter 2 | 8254 Counter 2       |
| Base+3  | Reserved       | 8254 Counter Control |

### 8254 Counter Control Word

| SC1            | SC0 | RW1        | RW0 | M2          | M1 | M0 | BCD |
|----------------|-----|------------|-----|-------------|----|----|-----|
| Select Counter |     | Read/Write |     | Mode Select |    |    | BCD |

## 2.3.11 A/D Input Buffer Register

(READ) Base+4 : A/D Low Byte Data Format

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |

(READ) Base+5 : A/D High Byte Data Format

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| D15   | D14   | D13   | D12   | D11   | D10   | D9    | D8    |

A/D 16 bits of data : D15.....D0, D15=MSB, D0=LSB

The low 8-bit A/D data are stored in address BASE+4 and the high 8-bit data are stored in address BASE+5.

### Ideal Input Voltages and Output Codes Table

| Description                 | Analog input | BINARY CODE         | HEX CODE |
|-----------------------------|--------------|---------------------|----------|
| Full Scale Range            | -10 ~ +10 V  |                     |          |
| Least Significant Bit (LSB) | 305 $\mu$ V  |                     |          |
| +Full Scale (10 V-1 LSB)    | 9.999695 V   | 0111 1111 1111 1111 | 7FFF     |
| Midscale                    | 0 V          | 0000 0000 0000 0000 | 00000    |
| One LSB below Midscale      | -305 $\mu$ V | 1111 1111 1111 1111 | FFFF     |
| - Full Scale                | -10 V        | 1000 0000 0000 0000 | 8000     |

---

## 2.3.12 D/A Output Latch Register

(WRITE) Base+4 : Channel 0 D/A Low Byte Data Format

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |

(WRITE) Base+5 : Channel 0 D/A High Byte Data Format

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| X     | X     | X     | X     | D11   | D10   | D9    | D8    |

(WRITE) Base+6 : Channel 1 D/A Low Byte Data Format

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |

(WRITE) Base+7 : Channel 1 D/A High Byte Data Format

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| X     | X     | X     | X     | D11   | D10   | D9    | D8    |

D/A 12 bits of output data : D11..D0, D11=MSB, D0=LSB, X= don't care

The D/A converter will convert the 12-bit digital data to analog output. The low 8-bit data of **D/A channel 0** are stored in address BASE+4 and high 4-bit data are stored in address BASE+5. The address BASE+6 and BASE+7 store the 12 bits of data for **D/A channel 1**. The D/A output latch registers are designed as a “**double buffered**” structure, so the analog output latch registers will be updated until the high 4 bits digital data are written. **The user must send low 8 bits first and then send high 4 bits to update the 12-bit AD output** latch register.

**NOTE : Send low 8 bits first, then send high 4 bits.**

---

## 2.3.13 D/I Input Buffer Register

(READ) Base+6 : D/I Input Buffer Low Byte Data Format

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |

(READ) Base+7 : D/I Input Buffer High Byte Data Format

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| D15   | D14   | D13   | D12   | D11   | D10   | D9    | D8    |

D/I 16 bits input data : D15..D0, D15=MSB, D0=LSB

The A-826PG provides 16 TTL compatible digital inputs. The low 8 bits are stored in address BASE+6. The high 8 bits are stored in address BASE+7.

## 2.3.14 Clear Interrupt Request

(WRITE) Base+8 : Clear Interrupt Request Format

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| X     | X     | X     | X     | X     | X     | X     | X     |

X=don't care, XXXXXXXX=any 8 bits data is validate

If A-826PG is working in the interrupt transfer mode, an on-board hardware status bit will be set after each A/D conversion. This bit must be **cleared by software** before next hardware interrupt. Writing any value to address BASE+8 will clear this hardware bit and the hardware will generate another interrupt when next A/D conversion is completed.

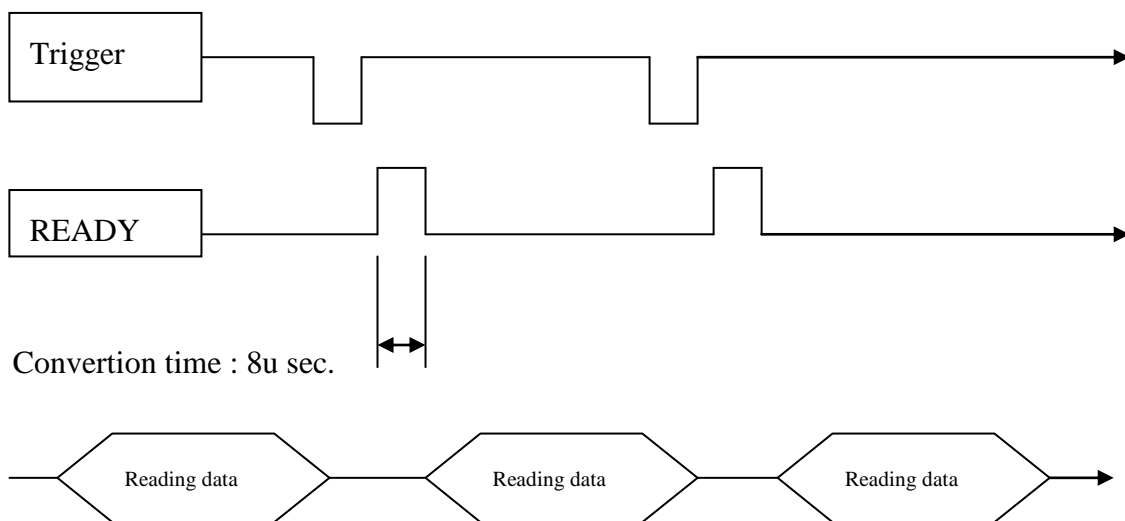
## 2.3.15 A/D Conversion Ready

(READ) Base+8 A/D Data Conversion Ready Format

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| X     | X     | X     | READY | X     | X     | X     | X     |

READY = 0 : A/D Conversion Ready

READY = 1 : A/D Conversion Not Ready



The READY bit is used as an indicator for A/D conversion. **When an A/D conversion is completed, the READY bit will be cleared to zero.**

---

## 2.3.16 A/D Gain Control Register

(WRITE) Base+9 : A/D Gain Control Register Format

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| X     | X     | X     | X     | X     | X     | GAIN1 | GAIN0 |

The **A-826PG** provides gain factor of 1/2/4/8

**NOTE** : **If the gain control code is changed, the hardware needs to delay extra gain settling time.** The gain settling time is different for different gain control code. **The software driver does not control the gain settling time, so the user must delay the gain settling time if the gain is changed.** If the application program needs to run in different machines, the user needs to implement a machine independent timer. The software driver, **A826\_delay()**, is designed for this purpose. If user uses this subroutine, the counter2 introduced in sec 2.6 is reserved by software driver to implement this machine's independent timer.

## A826PGL GAIN CONTROL CODE TABLE

| Settling Time | GAIN | Input Range | GAIN1 | GAIN0 |
|---------------|------|-------------|-------|-------|
| 23 $\mu$ s    | 1    | +/- 10 V    | 0     | 0     |
| 23 $\mu$ s    | 2    | +/- 5 V     | 0     | 1     |
| 25 $\mu$ s    | 4    | +/- 2.5 V   | 1     | 0     |
| 28 $\mu$ s    | 8    | +/- 1.25 V  | 1     | 1     |



## 2.3.17 A/D Multiplex Control Register

(WRITE) Base+A : A/D Multiplexer Control Register Format

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| X     | X     | X     | X     | D3    | D2    | D1    | D0    |

A/D input channel selection data = 4 bits : D3..D0, D3=MSB, D0=LSB, X=don't care

**Single-ended mode : D3..D0**

**Differential mode : D2..D0, D3= "X" (don't care)**

The A-826PG provides 16 single-ended or 8 differential analog input signals. In single-ended mode D3..D0 selects the active channel. In differential mode D2..D0 selects the active channel and D3 will be "X". (don't care)

**NOTE: The settling time of the multiplexer depends on the source resistance of input sources.**

**source resistance = about 0.1 kOhm → settling time = about 3 μs.**

**source resistance = about 1 kOhm → settling time = about 5 μs.**

**source resistance = about 10 kOhm → settling time = about 10 μs.**

**source resistance = about 100 kOhm → settling time = about 100 μs.**

## 2.3.18 A/D Mode Control Register

(WRITE) Base+B : A/D Mode Control Register Format

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| X     | X     | X     | X     | X     | D2    | D1    | D0    |

X=don't care

| JP5 Select Internal Trigger |    |    |               |            |               |           |        |
|-----------------------------|----|----|---------------|------------|---------------|-----------|--------|
| Mode Select                 |    |    | Trigger Type  |            | Transfer Type |           |        |
| D2                          | D1 | D0 | Software Trig | Pacer Trig | Software      | Interrupt | DMA    |
| 0                           | 0  | 0  | X             | X          | X             | X         | X      |
| 0                           | 0  | 1  | Select        | X          | Select        | X         | X      |
| 0                           | 1  | 0  | X             | Select     | X             | X         | Select |
| 1                           | 1  | 0  | X             | Select     | Select        | Select    | X      |

X=disable

| JP5 Select External Trigger |    |    |                  |               |           |        |
|-----------------------------|----|----|------------------|---------------|-----------|--------|
| Mode Select                 |    |    | Trigger Type     | Transfer Type |           |        |
| D2                          | D1 | D0 | External Trigger | Software      | Interrupt | DMA    |
| 0                           | 0  | 0  | X                | X             | X         | X      |
| 0                           | 0  | 1  | X                | X             | X         | X      |
| 0                           | 1  | 0  | Select           | X             | X         | Select |
| 1                           | 1  | 0  | Select           | Select        | Select    | X      |

The A/D conversion operation can be divided into 2 stages, **trigger stage and transfer stage**. The trigger stage will generate a trigger signal to the A/D converter and the transfer stage will transfer the result to the CPU.

The trigger method may be **internal trigger** or **external trigger**. The internal trigger can be **software trigger** or **pacemaker /event trigger**. **The software trigger is very simple but cannot control the sampling rate precisely.** In software trigger mode, the program issues a software trigger command any time needed. Then the program will poll the A/D status bit until the ready bit is 0.

**The pacemaker/event trigger can control the sampling rate very precisely. So the converted data can be used to reconstruct the wave form of the analog input signal.** In pacemaker trigger mode, the pacemaker timer will periodically generate trigger signals to the A/D converter. These converted data can be transfer to the CPU by polling or interrupt or DMA transfer method.

The software driver provides three data transfer methods, **polling, interrupt and DMA**. The polling subroutine, A826\_AD\_PollingVar() or A826\_AD\_PollingArray(), sets the A/D mode control register to **0x01**. This control word means software trigger and polling transfer. The interrupt subroutine, A826\_AD\_INT\_START(...), sets the A/D mode control mode register to **0x06**. This control word means pacemaker trigger and interrupt transfer. The DMA subroutine, A826\_AD\_DMA\_START(...), sets the A/D mode control register to **0x02**. This control word means pacemaker trigger and DMA transfer.

---

## 2.3.19 A/D Software Trigger Control Register

(WRITE) Base+C : A/D Software Trigger Control Register Format

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| X     | X     | X     | X     | X     | X     | X     | X     |

X=don't care, XXXXXXXX=any 8 bits data is validate

The A/D converter can be triggered by software trigger or pacer trigger. Writing any value to address BASE+C will generate a trigger pulse to A/D converter and initiated an A/D conversion operation. The address BASE+8 offers a ready bit to indicate an A/D conversion has been complete.

The software driver uses this control word to detect the A-826PG hardware board. **The software initiates a software trigger and checks the ready bit.** If the ready bit can not be cleared to zero in a fixed time, the software driver will return an error message. If the I/O BASE address setting error, the ready bit will not be clear to zero. The software driver, **A826\_CheckAddress()**, uses this method to detect the of the I/O BASE address setting

---

## 2.3.20 D/O Output Latch Register

(WRITE) Base+D : D/O Output Latch Low Byte Data Format

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |

(WRITE) Base+E : D/O Output Latch High Byte Data Format

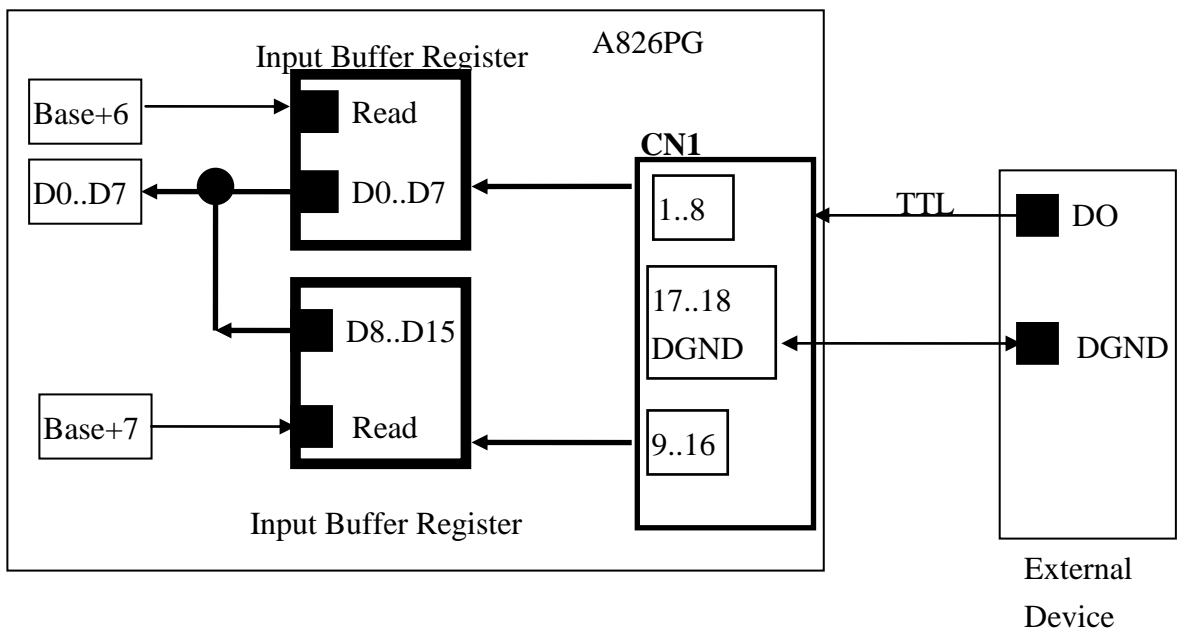
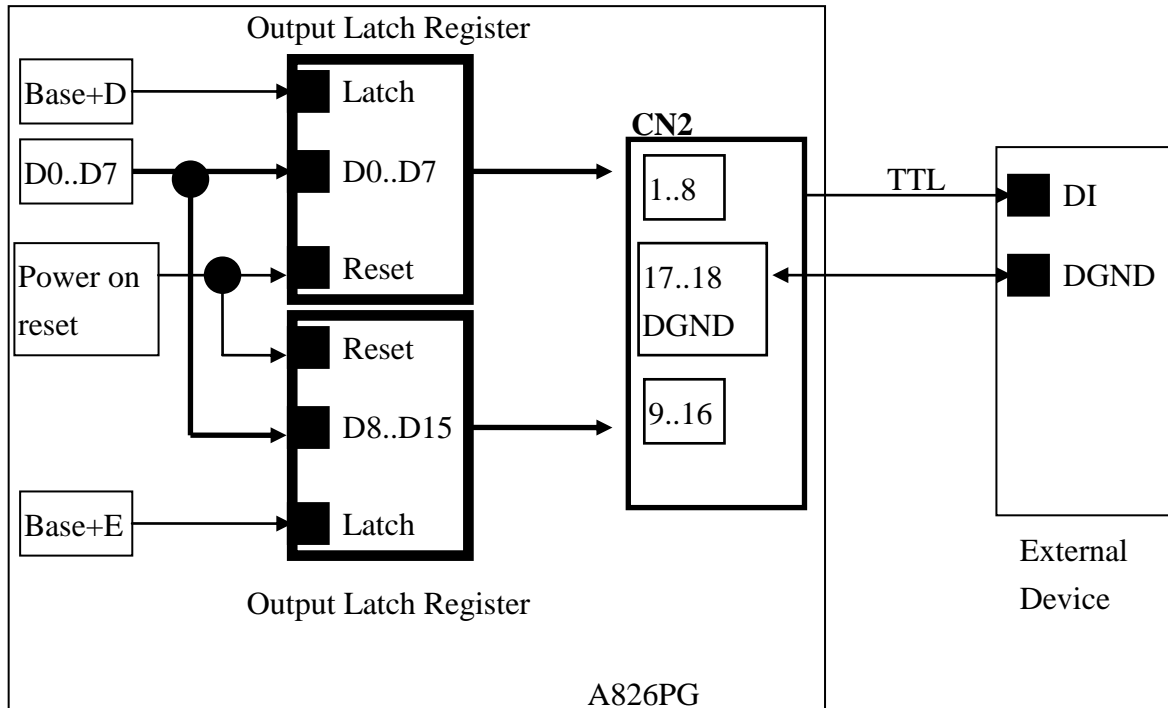
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| D15   | D14   | D13   | D12   | D11   | D10   | D9    | D8    |

D/O 16 bits output data : D15..D0, D15=MSB, D0=LSB

The A-826PG provides 16 TTL compatible digital outputs. The low 8 bits are stored in address **BASE+D**. The high 8 bits are stored in address **BASE+E**

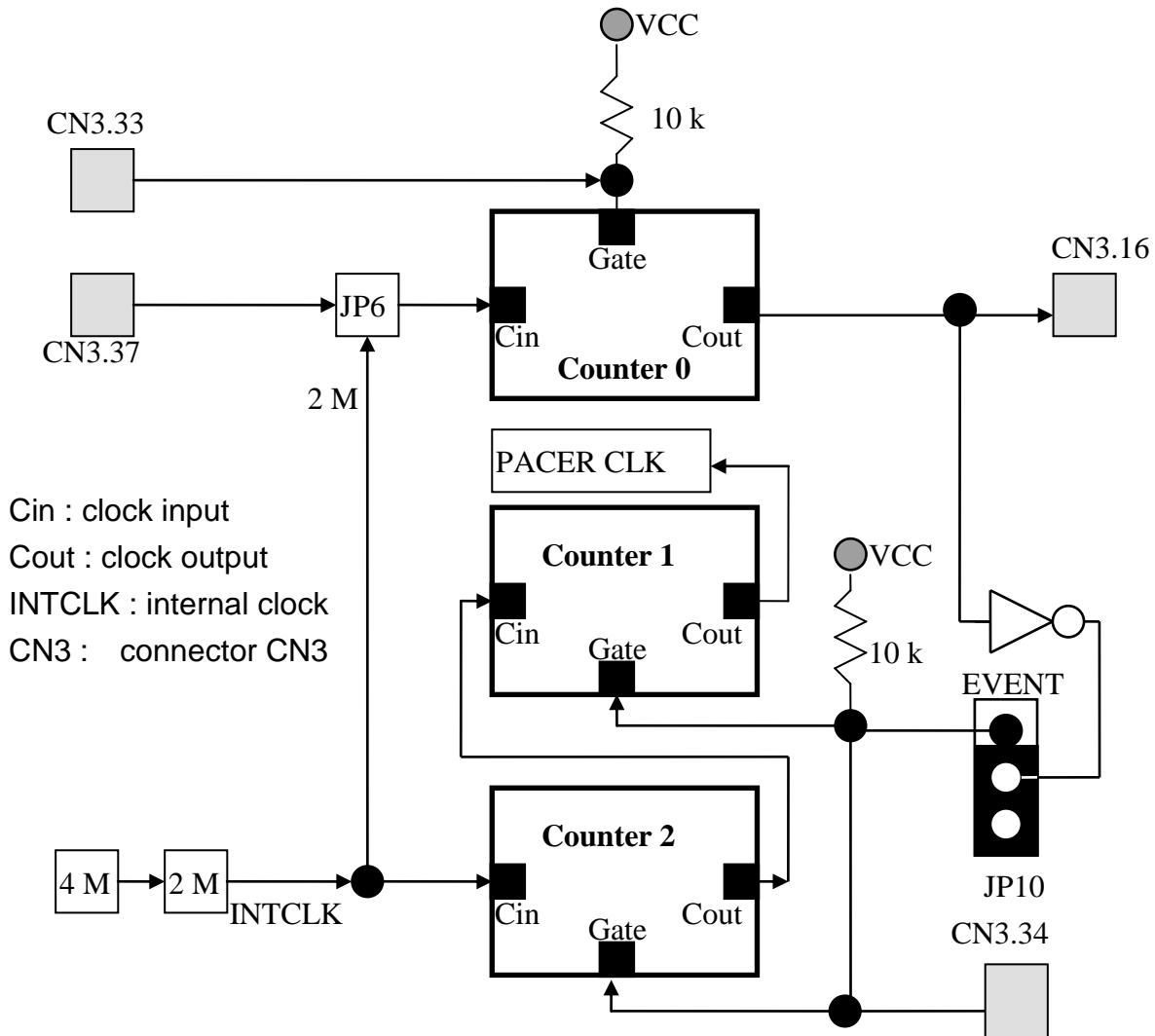
## 2.4 Digital I/O

The A-826PG provides 16 digital input channels and 16 digital output channels. All signal levels are TTL compatible. The connections diagram and block diagram are given below:



## 2.5 8254 Timer/Counter

The 8254 Programmable timer/counter has 4 registers from Base+0 through Base+3. For detailed programming information about the 8254, please refer to Intel's "Microsystem Components Hand book". The block diagram is as below.



Counter0, counter1 and counter2 are all 16 bits counter. Counter 1 and counter 2 cascade as a 32-bit timer. This 32-bit timer is used as a **pacemaker timer**. The software driver, **A826\_Delay()**, uses counter 0 to implement a machine independent timer for settling time delay. If users don't use A826\_Delay(), counter0 can be used as a general purpose timer/counter.

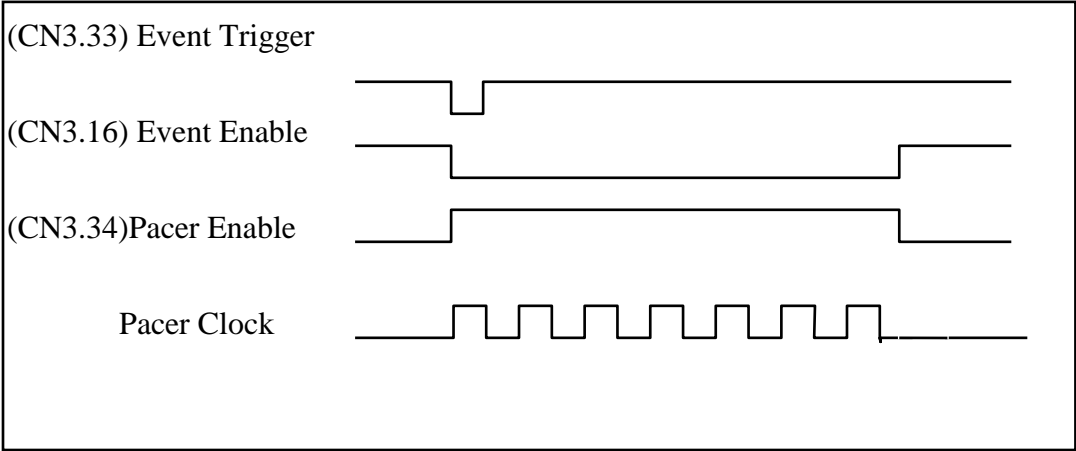
**NOTE :** When users call **A826\_Delay()** to implement a machine independent timer, the JP6 must select internal 2 M clock.

The counter 0 can be used to implement an event trigger controller. The user can send an event signal to CN3.33 to generate a START\_CONVERT (CN3.16) signal. This START\_CONVERT signal will enable the pacer timer (counter 1 & counter 2) to generate one pacer trigger signal which will feed into the A/D converter to initiate an A/D conversion cycle. The machine independent timer also uses timer/counter 0, so the user cannot use both the machine independent timer and the event trigger controller at the same time. If the user wants to use the event trigger controller, the JP10 must select in the correct position... In default condition, the JP10 is set in the disable event trigger position.

The “hardware retriggerable one-shot mode” of 8254 (mode 1) can be used to implement this event trigger controller. The event signal will be in the HIGH signal level in the initial condition. . After the control codes are written into the 8254 control register, the CN3.16 (Cout) will go into HIGH signal level. This HIGH signal will be inverted into the GATE input of the pacer timer (CN3.34). So the pacer timer will be in the disable state and can not generate any pacer clock output.

When the event signal go to the LOW signal level, the CN3.16(Cout) will go to the LOW signal level. **The interval of LOW signal is called the one shot period and can be programmable by control word.** This LOW level interval signal will be inverted to enable the pacer timer to generate pacer trigger signal. **So the period of LOW level signal must be long enough to generate the desired pacer clocks.**

The event trigger controller only generate **ENABLE** signal and must be used with the pacer trigger. If the user only use event trigger controller, the hardware will generate only enable signal (missed trigger signal).



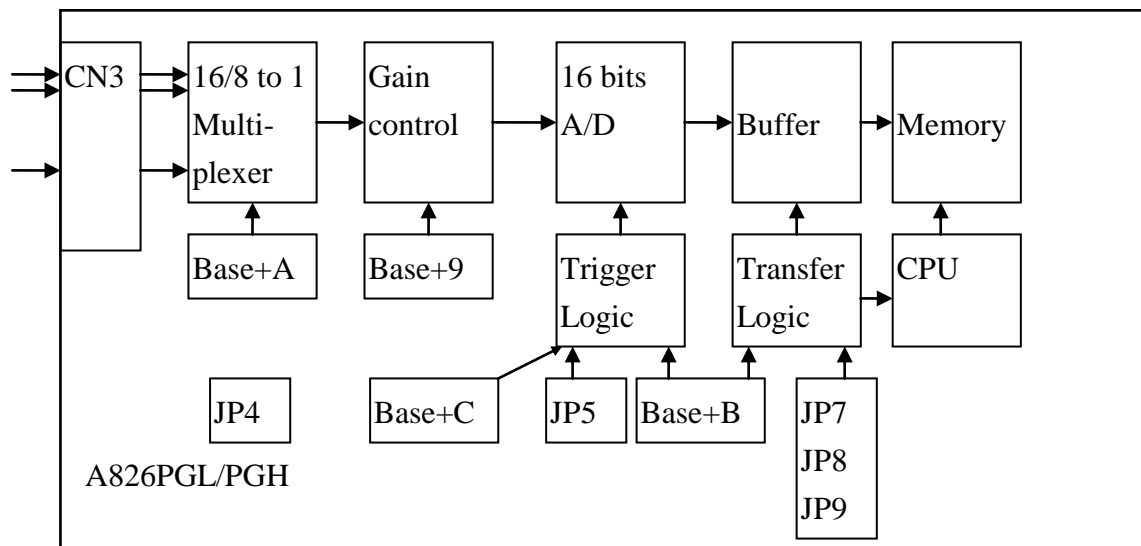
## 2.6 A/D Conversion

A/D conversion can be initiated in one of three ways: software command, internal programmable interval timer or external trigger to the A/D. At the end of the A/D conversion, it is possible to transfer the data by one of three ways: polling a status register and reading data when ready, generating hardware interrupt and an interrupt service routine, or through DMA (direct Memory Access). All operating modes are selected by a control register on the A-826PG and are supported by the utility software.

Before use the A/D conversion function, user should notice the following issue:

- \* A/D data register, BASE+4/BASE+5, store the A/D conversion data.
- \* A/D data conversion ready register, (BASE +8) checks A/D conversion ready.
- \* A/D gain control register, BASE+9, selects gain.
- \* A/D multiplex control register, BASE+A, selects analog input.
- \* A/D mode control register, BASE+B, selects trigger type and transfer type.
- \* A/D software trigger control register, BASE+C.
- \* JP4 selects single-ended or differential input.
- \* JP5 selects internal/external trigger.
- \* JP7 selects IRQ level.
- \* JP6 selects internal/external clock for counter0.
- \* JP8,JP9 selects DMA channel.
- \* **3 trigger logic : software, pacer, external trigger.**
- \* **3 transfer logic : polling, interrupt, DMA.**

The block diagram is given below:..





---

## 2.6.1 A/D conversion flow

Before using the A/D converter, the user should setup the following hardware items:

1. Selects single-ended or differential input (JP4).
2. Selects internal trigger or external trigger (JP5).
3. Selects IRQ level if needed (JP7).
4. Selects DMA channel if needed (JP8, JP9).
5. Selects internal clock or external clock for counter0 if needed (JP6).

The software driver supports three different modes: **polling, interrupt and DMA**. The user can control the A/D conversion by polling mode very easy. It is recommended to use the software driver if using interrupt or DMA mode.

The analog input signals come from CN3. These signals may be single-ended or differential type and must match with the setting of JP3.

The multiplexer can select 16 single-ended or 8 differential signals into the gain control module. **The settling time of multiplexer depends on the impedance of the signal source.** Because the software **doesn't manage the settling time, the user should delay enough settling time when the AD channel changes.**

The gain control module also need settling time if gain control code changed. Because the software **doesn't control the settling time, the user should delay enough settling time to accommodate for gain control code changes.**

The software driver provides a **machine independent timer, A826\_Delay()**, for settling time delay. This subroutine assumes that JP6 select internal 2 M clock and uses counter0 to implement a machine independent timer. If the user call A826\_delay(), the counter0 will be reserved and can't be used as a user programmable timer/counter.

The output of the gain control module feeds into the A/D converter. **The A/D converter needs a trigger signal to start an A/D conversion cycle.** The A-826PG supports four trigger modes **software, pacer, event and external trigger.**

---

## 2.6.2 A/D Conversion Trigger Modes

A-826PG supports three trigger modes.

### **1 : Software Trigger :**

Write any value to A/D software trigger control register, BASE+A, will initiate an A/D conversion cycle. This mode is very simple but very difficult to control sampling rate.

### **2 : Pacer Trigger Mode :**

The block diagram of pacer timer is show in section 2.6. The sample rate of pacer is very precise.

### **3 : External Trigger Mode :**

When a rising edge of external trigger signal is applied, a A/D conversion will be performed. The external trigger source comes from pin 17 of CN3.

### **4 : Event Trigger Mode:**

When the event signal goes from HIGH to LOW, the event trigger controller will generate an programmable **ENABLE** interval to enable the pacer trigger. So this mode must be used with the pacer trigger mode.

---

## 2.6.3 A/D Transfer Modes

A-826PG supports three transfer modes.

### **1 : polling transfer :**

This mode can be used with all trigger modes. Detailed information is given in section 2.4.8. The software scans A/D high byte data register, BASE+5, until Data Ready Register Base +8 READY\_BIT=0.The low byte data is also ready in BASE+4.

### **2 : interrupt transfer :**

This mode can be used with pacer trigger or external trigger. Detailed information is given in section 2.4.8.The user can set the IRQ level by adjusting JP7. A hardware interrupt signal is sent to the PC when an A/D conversion is completed.

### **3 : DMA transfer :**

This mode can be used with pacer trigger or external trigger. Detailed information is given in section 2.4.8. The user can set the DMA channel by adjusting JP8, JP9. Two hardware DMA requests signal are sent sequentially to the PC when an A/D conversion is completed. The single mode transfer of 8237 is suggested.

**If using interrupt or DMA transfer, it is recommended to use A826 software driver.**

---

## 2.6.4 Software trigger and polling technique

The simplest way to control as following steps :

1. sends 0x01 to A/D mode control register (software trigger + polling transfer)
2. sends channel number to multiplexer control register
3. sends the gain control code value to gain control register.
4. sends any value to software trigger control register to generate a software trigger signal.
5. scans the READY bit of the A/D high byte data until READY=0
6. reads the 16-bit A/D data
7. converts this 16-bit binary data to the floating point value

Example: (QBasic Language)

```
Bas=&h220           'Set Base Address in 220 HEX
OUT Bas+11,0        'Set Soft Trigger Mode
OUT Bas+9.,0        'Set Gain=1 , Input Range = ±10
OUT Bas+10,0        'Set A/D Channel 0

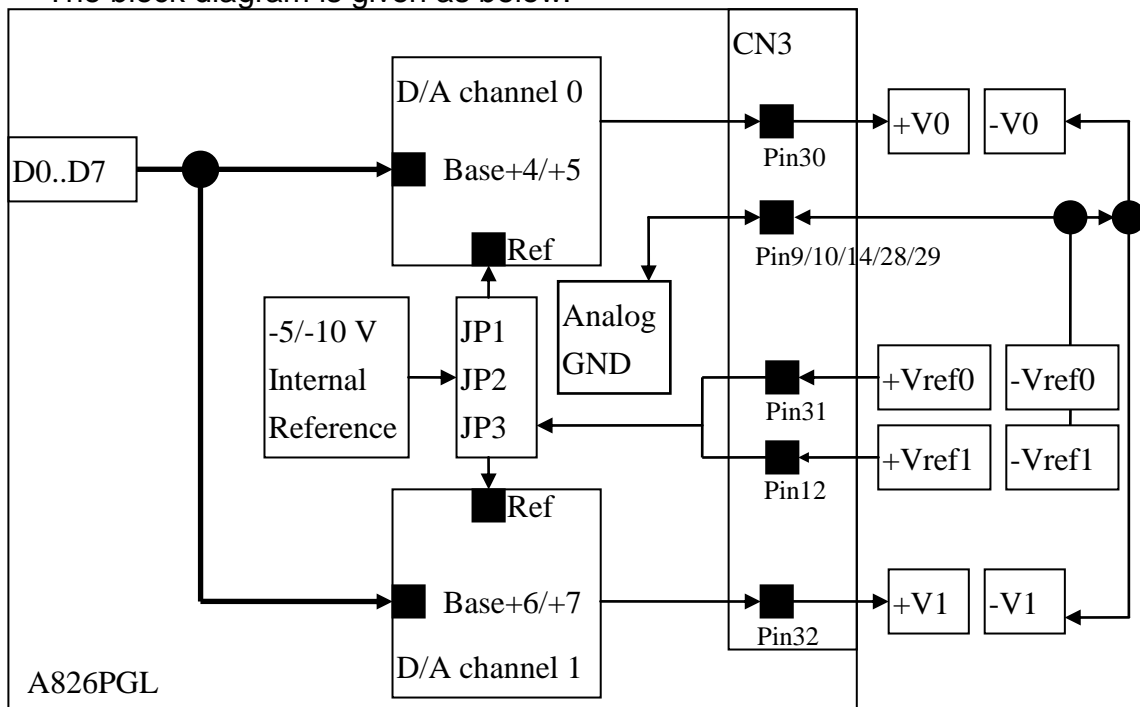
OUT Bas+12,0        'Send A/D Soft Trigger
DRDY=1
WHILE DRDY=1
    DRDY=Inp(Bas+8)    'Check DRDY = 0 Then A/D Conversion O.K
    CONVEROK=DRDY AND &H20
    If CONVEROK=0 then DRDY=1 Else DRDY=0
WEND
MSB= Inp(Bas+5)      'Read A/D High Byte
LSB = Inp(Bas+4)     'Read A/D Low Byte
Addata=MSB*256+LSB   'Conversion Binary Code to Voltage Value
If Addata >= &h8000 and Addata <= &hFFFF THEN Addata =65535-Addata
Vin = Addata * 10 / 32768
```

## 2.7 D/A Conversion

The A-826PG provides two 12 bits D/A converters. Before using the D/A conversion function, user should notice the following issue:

- DA output register, BASE+4/BASE+5/BASE+6/BASE+7. (see [Section 2.3.12](#))
- JP1 is used to select internal reference voltage -5 V or -10 V (see [Section 2.3.1](#)).
- JP2/JP3 is used to select internal or external reference voltage (see [Section 2.3.2](#)).
  - ⇒ If **JP2/JP3** selects **internal** and **JP1** select **-5 V**, the DA output range from **0 to +5 V<sub>DC</sub>**.
  - ⇒ If **JP2/JP3** selects **internal** and **JP1** select **-10 V**, the DA output range from **0 to +10 V<sub>DC</sub>**.
  - ⇒ If **JP2/JP3** selects **external**, the **ExtRef0 (CN3 pin 31)/ExtRef1 (CN3 pin 12)** connected to **external voltage -10 V<sub>DC</sub> to +10 V<sub>DC</sub>**, the D/A output range as follows:
    - External Reference Voltage +10 V<sub>DC</sub> (Max.) → the DA output range from **0 to -10 V<sub>DC</sub>**.
    - External Reference Voltage -10 V<sub>DC</sub> (Max.) → the DA output range from **0 to +10 V<sub>DC</sub>**.

The block diagram is given as below:



NOTE : The DA output latch registers are designed as “double buffer” structure. **The user must send the low byte data first, and then send the high byte data to store the DA 12-bit digital data.** If the user only sends the high byte data, then the low byte data will still be the previous value. Also, if the user sends high byte first then sends low byte, the low byte data of DA is still held in the previous one.

---

## 2.8 Analog Input Signal Connection

The A-826PG can be used to measure single-ended or differential type analog input signals. Some analog signals can be measured in both single-end and differential mode, but some can only be measured in either single-ended or differential mode. The user must decide which mode is suitable for measurement.

In general, there are 3 different analog signal connection methods as shown in Fig1 to Fig3. Fig1 is suitable for grounding source analog input signals. Fig2 can measure more channels than Fig1, but is only suitable for large analog input signals. Fig3 is suitable for thermocouple and Fig4 is suitable for floating source

**Note : In Fig3, the maximum common mode voltage between the analog input source and the AGND is 70 V<sub>p-p</sub>, If the common mode voltage is over 70 V<sub>p-p</sub>, the input multiplexer will be damaged forever.**

The simple way to select the input signal connection configuration is as below.

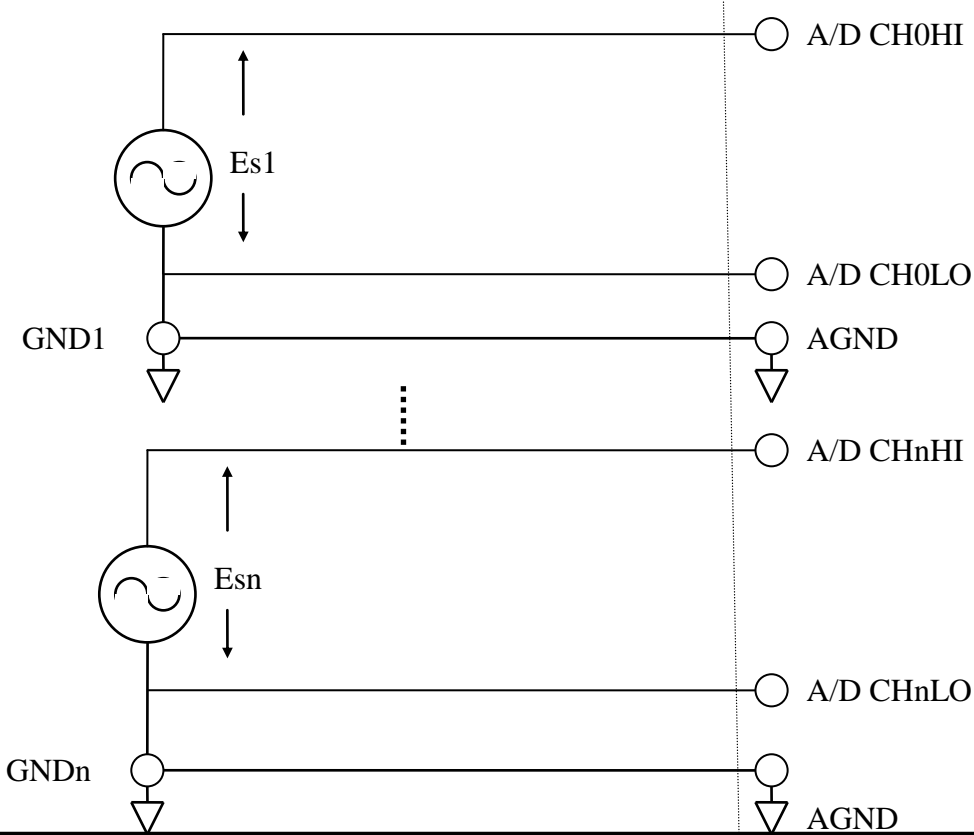
- 1. Grounding source input signal      → select Fig1**
- 2. Thermocouple input signal      → select Fig3**
- 3. Floating source input signal      → select Fig4**
- 4. If V<sub>in</sub> > 0.1 V and gain ≤ 10 and need more channels  
   → select Fig2**

If the user isn't able to determine the characteristics of the input signal, the test steps are given as below:

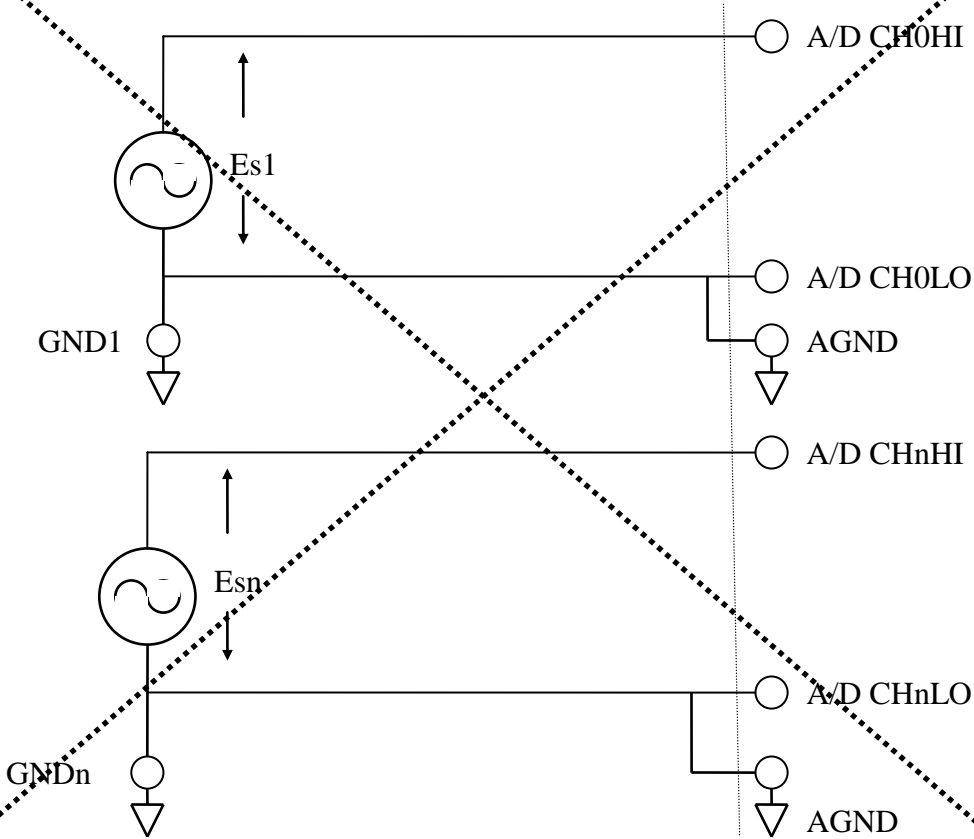
- 1. Step1 : try Fig1 and record the measurement results**
- 2. Step2 : try Fig4 and record the measurement results**
- 3. Step3 : try Fig2 and record the measurement results**
- 4. Compare the measurement results of step1,step2,step3  
and select the best one**

**1. FG1 : Connecting grounding source input (Right way)**

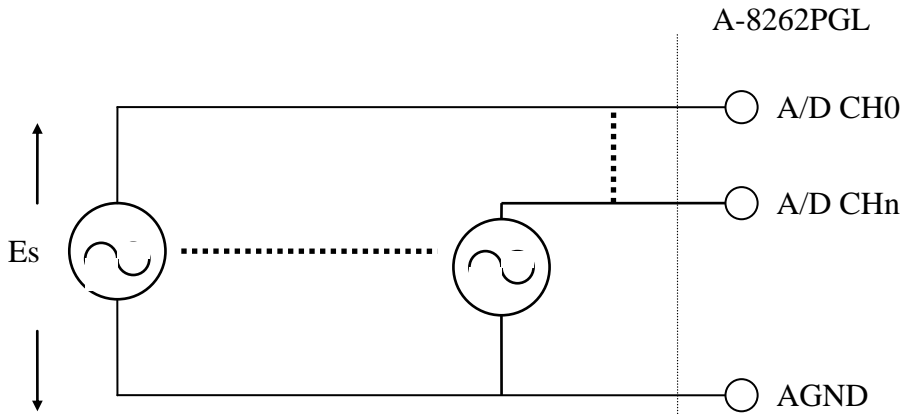
A-826PG



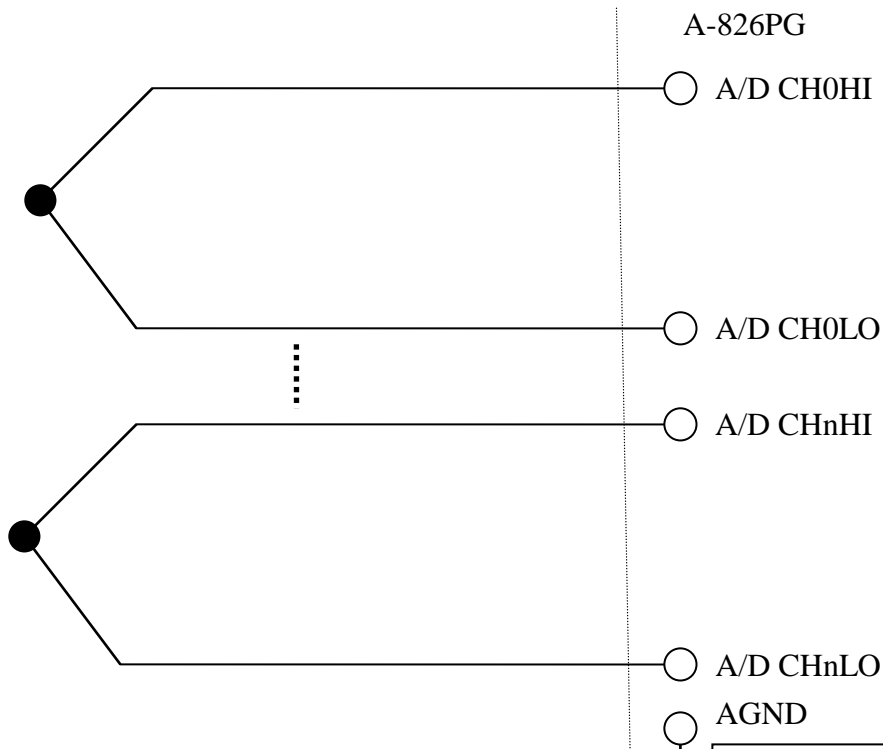
**FG1 : Wrong way**



**FG2 : Connecting singled-ended input**



**FG3 : connecting to thermocouple input**

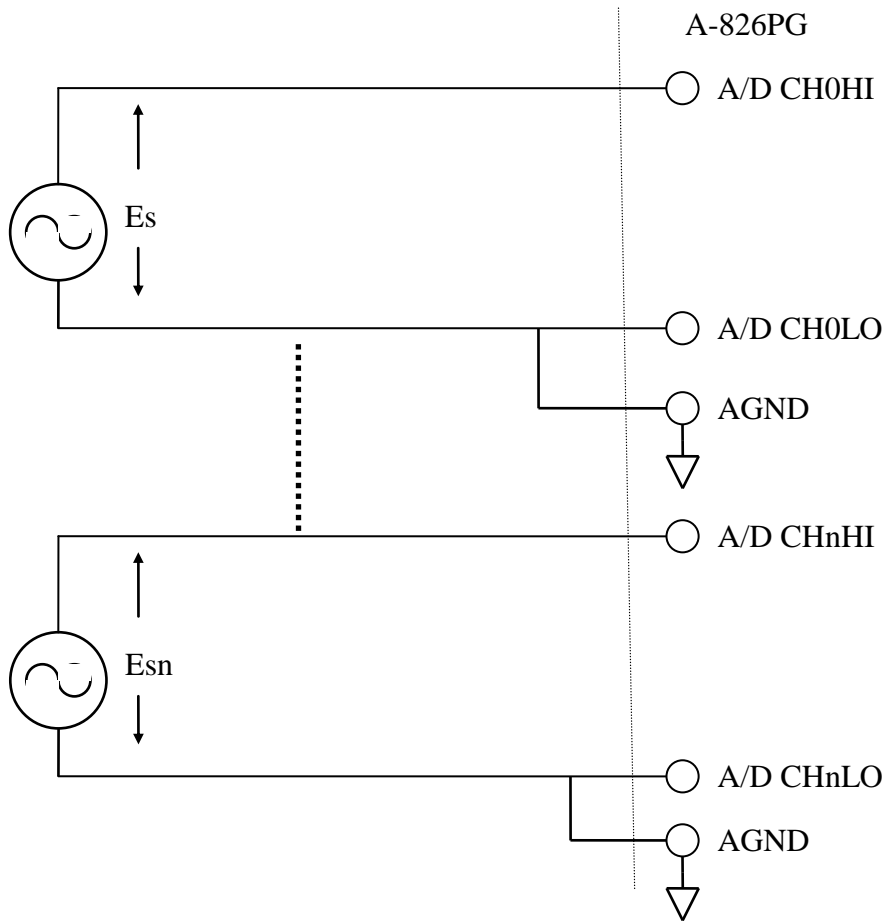


**Note :** If the input signal is not thermocouple, the user should use oscilloscope to measure common mode voltage of  $V_{in}$  before connecting to A-826PG. Don't use voltage meter or multimeter.

Do not join LO to AGND at the computer

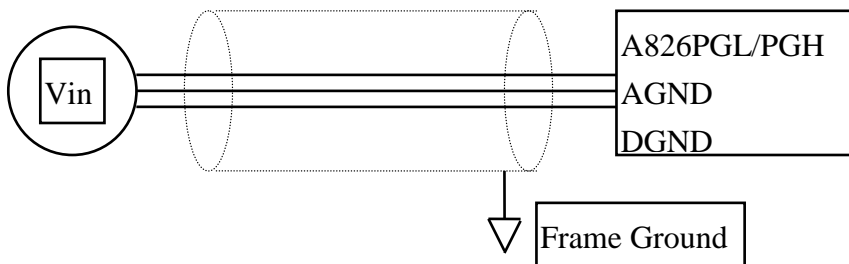
**CAUTION:** In Fig3, the maximum common mode voltage between the analog input source and the AGND is  $70 V_{p-p}$ . If the common mode voltage is over  $70 V_{p-p}$ , the input multiplexer will be damaged forever.

## FG4 : connecting to floating signal source input



## Signal Shielding

- \* Signal shielding connections in Fig1 to Fig4 are all the same
- \* Use single-point connection to **frame ground (not AGND or DGND)**





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## 2.9 Using DB-8225 CJC Output

The CJC Circuitry on DB-8225 is used to produce 10mV per Deg C With 0.0 Volts @ -273 Deg C. The A-826 should be protected from draughts and direct sunlight in order to accurately reflect room temperature.

### CJC Calibration:

1. Connects the A-826PG to DB-8225 CN1
2. Sets the A-826PG to Single-ended Mode
3. Sets the DB-8225 JP1 to 1-2 and JP2 to 2-3 ( Single-ended mode)
4. Reads the temperature from a digital thermometer placed near D1/D2 (See DB-8265 Layout) .
5. Reads the A-826PG analog input channel 0 (single-ended Channel 0)
6. Adjusts VR1 until a stable reading of 10 mV per deg C is attained.

For example, when the environment temperature is 24 °C. the reading value of CJC will be 2.97 V

$$(273\text{ }^{\circ}\text{C} + 24\text{ }^{\circ}\text{C}) \times 10\text{ mV}/^{\circ}\text{C} = 2.97\text{ V}$$

You should use an A/D Channel for CJC calibration. AI0 is reserved for the CJC calibration used in single ended mode and CH0-HI & CH0-LO are reserved for differential mode. It is recommended to use differential mode if measuring thermocouple.

---

## 3. Pin Assignments

The A-826PG provides three connectors. Connector 1, **CN1, functions as 16-bit digital input.** Connector 2, **CN2, functions as a 16-bit digital output.** Connector 3, **CN3, functions as analog input, analog output or timer/counter input/output.**

---

### 3.1 CN1/CN2/CN3 Pin Assignment

**CN1 : Digital Input Connector Pin Assignment.**

| Pin Number | Description          | Pin Number | Description          |
|------------|----------------------|------------|----------------------|
| 1          | Digital Input 0/TTL  | 2          | Digital Input 1/TTL  |
| 3          | Digital Input 2/TTL  | 4          | Digital Input 3/TTL  |
| 5          | Digital Input 4/TTL  | 6          | Digital Input 5/TTL  |
| 7          | Digital Input 6/TTL  | 8          | Digital Input 7/TTL  |
| 9          | Digital Input 8/TTL  | 10         | Digital Input 9/TTL  |
| 11         | Digital Input 10/TTL | 12         | Digital Input 11/TTL |
| 13         | Digital Input 12/TTL | 14         | Digital Input 13/TTL |
| 15         | Digital Input 14/TTL | 16         | Digital Input 15/TTL |
| 17         | PCB's GND output     | 18         | PCB's GND output     |
| 19         | PCB's +5 V output    | 20         | PCB 's +12 V output  |

**CN2 : Digital Output Connector Pin Assignment.**

| Pin Number | Description           | Pin Number | Description           |
|------------|-----------------------|------------|-----------------------|
| 1          | Digital Output 0/TTL  | 2          | Digital Output 1/TTL  |
| 3          | Digital Output 2/TTL  | 4          | Digital Output 3/TTL  |
| 5          | Digital Output 4/TTL  | 6          | Digital Output 5/TTL  |
| 7          | Digital Output 6/TTL  | 8          | Digital Output 7/TTL  |
| 9          | Digital Output 8/TTL  | 10         | Digital Output 9/TTL  |
| 11         | Digital Output 10/TTL | 12         | Digital Output 11/TTL |
| 13         | Digital Output 12/TTL | 14         | Digital Output 13TTL  |
| 15         | Digital Output 14/TTL | 16         | Digital Output 15/TTL |
| 17         | PCB's GND output      | 18         | PCB's GND output      |
| 19         | PCB's +5 V output     | 20         | PCB's +12 V output    |

### 3.1.1 FOR SINGLE-ENDED SIGNAL

**CN3 : Analog input/Analog output/Timer/Counter Connector Pin Assignment.**

| Pin Number | Description  | Pin Number | Description  |
|------------|--|------------|--|
| 1          | Analog Input 0/+                                   | 20         | Analog Input 8/+   |
| 2          | Analog Input 1/+                                   | 21         | Analog Input 9/+   |
| 3          | Analog Input 2/+                                   | 22         | Analog Input 10/+  |
| 4          | Analog Input 3/+                                   | 23         | Analog Input 11/+  |
| 5          | Analog Input 4/+                                   | 24         | Analog Input 12/+  |
| 6          | Analog Input 5/+                                   | 25         | Analog Input 13/+  |
| 7          | Analog Input 6/+                                   | 26         | Analog Input 14/+  |
| 8          | Analog Input 7/+                                   | 27         | Analog Input 15/+  |
| 9          | PCB's analog GND output                            | 28         | PCB's analog GND output                                  |
| 10         | PCB's analog GND output                            | 29         | PCB's analog GND output                                  |
| 11         | D/A's internal -5 V/-10 V voltage reference output | 30         | D/A channel 0's analog voltage output                    |
| 12         | D/A channel 1's external voltage reference input   | 31         | D/A channel 0's external voltage reference input         |
| 13         | PCB's +12 V output                                 | 32         | D/A channel 1's analog voltage output                    |
| 14         | PCB's analog GND output                            | 33         | User timer/counter's GATE control input                  |
| 15         | PCB's digital GND output                           | 34         | Timer/counter 1&2's GATE control input                   |
| 16         | User timer/counter's output                        | 35         | Reserved   |
| 17         | External trigger source input/TTL                  | 36         | Reserved   |
| 18         | Reserved   | 37         | User timer/counter's external clock input (internal=2 M) |
| 19         | PCB's +5 V output                                  | XXXXXXX    | This pin not available                                   |

## 3.1.2 FOR DIFFERENTIAL SIGNAL

**CN3 : Analog input/Analog output/Timer/Counter Connector Pin Assignment.**

| Pin Number | Description  | Pin Number | Description  |
|------------|--|------------|--|
| 1          | Analog Input 0/+                                   | 20         | Analog Input 0/-   |
| 2          | Analog Input 1/+                                   | 21         | Analog Input 1/-   |
| 3          | Analog Input 2/+                                   | 22         | Analog Input 2/-   |
| 4          | Analog Input 3/+                                   | 23         | Analog Input 3/-   |
| 5          | Analog Input 4/+                                   | 24         | Analog Input 4/-   |
| 6          | Analog Input 5/+                                   | 25         | Analog Input 5/-   |
| 7          | Analog Input 6/+                                   | 26         | Analog Input 6/-   |
| 8          | Analog Input 7/+                                   | 27         | Analog Input 7/-   |
| 9          | PCB's analog GND output                            | 28         | PCB's analog GND output                                  |
| 10         | PCB's analog GND output                            | 29         | PCB's analog GND output                                  |
| 11         | D/A's internal -5 V/-10 V voltage reference output | 30         | D/A channel 0's analog voltage output                    |
| 12         | D/A channel 1's external voltage reference input   | 31         | D/A channel 0's external voltage reference input         |
| 13         | PCB's +12 V output                                 | 32         | D/A channel 1's analog voltage output                    |
| 14         | PCB's analog GND output                            | 33         | User timer/counter's GATE control input                  |
| 15         | PCB's digital GND output                           | 34         | Timer/counter 1&2's GATE control input                   |
| 16         | User timer/counter's output                        | 35         | Reserved   |
| 17         | External trigger source input/TTL                  | 36         | Reserved   |
| 18         | Reserved   | 37         | User timer/counter's external clock input (internal=2 M) |
| 19         | PCB's +5 V output                                  | XXXXXXX    | This pin not available                                   |

---

## 3.2 Daughter Board

The A-826PG can be connected with many different daughter boards. The function of these daughter boards are described as follows.

---

### 3.2.1 DB-8225

The DB-8225 (or ACLD-8125 series) provides a **on-board CJC** (Cold Junction Compensation) circuit for thermocouple measurement and **terminal block** for easy signal connection and measurement. The CJC is connected to A/D channel\_0. The A-826PG can connect CN3 direct to DB-8225 or equivalent (ACL-8125) through a 37-pin D-sub connector.

---

### 3.2.2 DB-37

The DB-37 (or ACLD-9137) is a **general purpose** 37-pin connector. This board directly connects to a 37-pin D-sub connector. It is suitable for easy signal connection and measurement.

---

### 3.2.3 DB-16P

The DB-16P (or 782 series) is a **16-channel isolated digital input** board. The A-826PG provides 16-channel non-isolated TTL-compatible digital inputs from CN1. If connecting to DB-16P, the A-826PG can provide 16-channel isolated digital input signals.

---

### 3.2.4 DB-16R

The DB-16R (or 782 series) provides **16-channel SPDT relay output**. The A-826PG provides 16-channel TTL-compatible digital output from CN2. If connected to the DB-16R, the A-826PG can provide 16-channel relay output to control power devices.

---

## 4. Calibration

The A-826PG is calibrated to its best state of operation. For environments with large vibration, recalibration is recommended. Before calibrating the A-826PG, user should takes care the following issues:

- \* One 6-digit multimeter
- \* One stable voltage source (4.9988 V)
- \* Diagnostic program : this program included in the delivered package will guide the user in further calibration.

---

### 4.1 Calibration VR Description

There are seven VRs on the A-826PG. Calibration needs to adjust all seven VRs.

| VR Num. | Description                                    |
|---------|--|
| VR1     | A/D's gain adjustment                          |
| VR2     | A/D's off-set adjustment                       |
| VR3     | D/A reference voltage adjustment               |
| VR4     | A/D programmable amplifier's offset adjustment |
| VR5     | D/A channel 0's gain adjustment                |
| VR6     | D/A channel 1's gain adjustment                |

---

## 4.2 D/A Calibration Steps

1. Run A82XDIAG.EXE
2. Press “Right Arrow Key” to select “CALIBRATION” item
3. Press “Down Arrow Key” to select “G. D/A REFERENCE” item.
4. Press “Enter Key”
5. Connect VREF, pin 11 of CN3, to DVM (DC Voltage Meter)
6. Adjust VR3 until DVM=4.9988 V
7. Press “ESC Key”
8. Select & Execute “A. D/A REFERENCE 1” item
9. Connect D/A channel 0, pin 30 of CN3, to DVM
10. Adjust VR5 until DVM=4.9988 V
11. Press “ESC Key”
12. Select & Execute “B. D/A REFERENCE2” item
13. Connect D/A channel 1, pin 32 of CN3, to DVM
14. Adjust VR6 until DVM=4.9988 V

---

## 4.3 A/D Calibration Steps

1. Run A82XDIAG.EXE
2. Press “Right Arrow Key” to select “CALIBRATION” item
3. Press “Down Arrow Key” to select “C. A/D REFERENCE” item.
4. Press “Enter Key”
5. Input stable 9.9997 V to A/D channel 0, pin 1 of CN3
6. Adjust VR1 until A/D data shown in screen between 32765 to 32767
7. Press “ESC Key”
8. Select & Execute “D. A/D OFFSET” item
9. Input stable 0 V to A/D channel 0, pin1 of CN3
10. Adjust VR1 until A/D data shown in screen between - 1 to + 1
11. Press “ESC Key”
12. Repeat step\_3 to step\_11 until no need to adjust VR2,VR1
13. Select & Execute “E. PGA OFFSET” item
14. Input stable 0 V to A/D channel 0, pin 1 of CN3
15. Adjust VR6 until A/D data shown in screen between - 1 to + 1
16. Press “ESC Key”

---

## 5. Diagnostic Utility

---

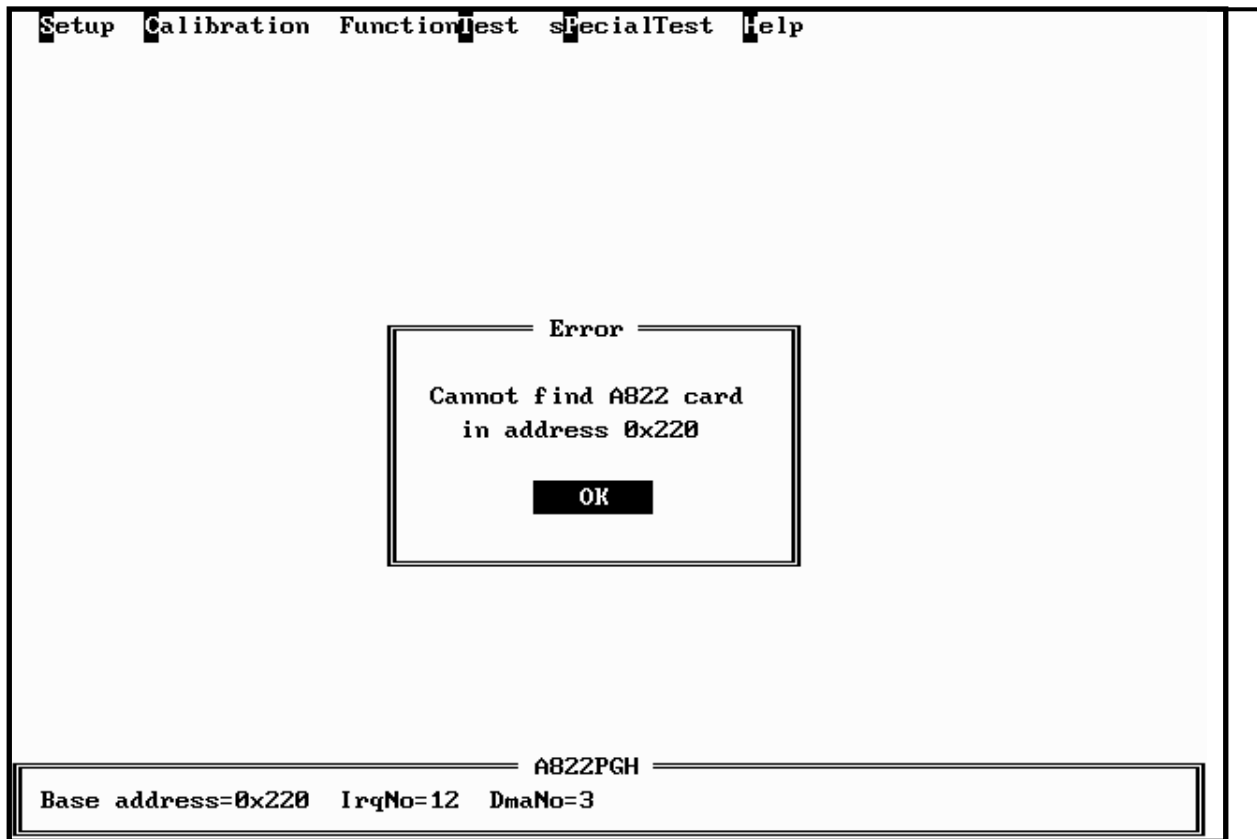
### 5.1 Introduction

The diagnostic utility, A82XDIAG.EXE, is a menu-driven program which assists the user in a complete testing of the A-826PG board. When in doubt regarding the operation of the A-826PG board, run the diagnostic utility to check the functions of the board. To run the diagnostic utility, change to the subdirectory used in the installation process (C:\A826 for example). Then type "A82XDIAG" <Enter> to start. The steps are shown as following:

```
C:\>CD A826 <Enter>
C:\A826>CD DIAG <Enter>
C:\A826\DIAG>A82XDIAG <Enter>
```

A configuration file, named A82X.CFG, is associated with the A82XDIAG.EXE. The configuration of the A-826PG board is recorded in this file. The information includes the I/O base address, interrupt number and DMA channel number used by the A-826PG. While the A82XDIAG is running, if you make some adjustments, the changes will not be saved automatically. Therefore, the user must select the save function to save the changes. When A82XDIAG.EXE starts up, it will automatically check if the jumper setting of the I/O base address is identical to the value stored in configuration file. If the address is not identical, an error message will appear to warn you. The screen is shown as below.



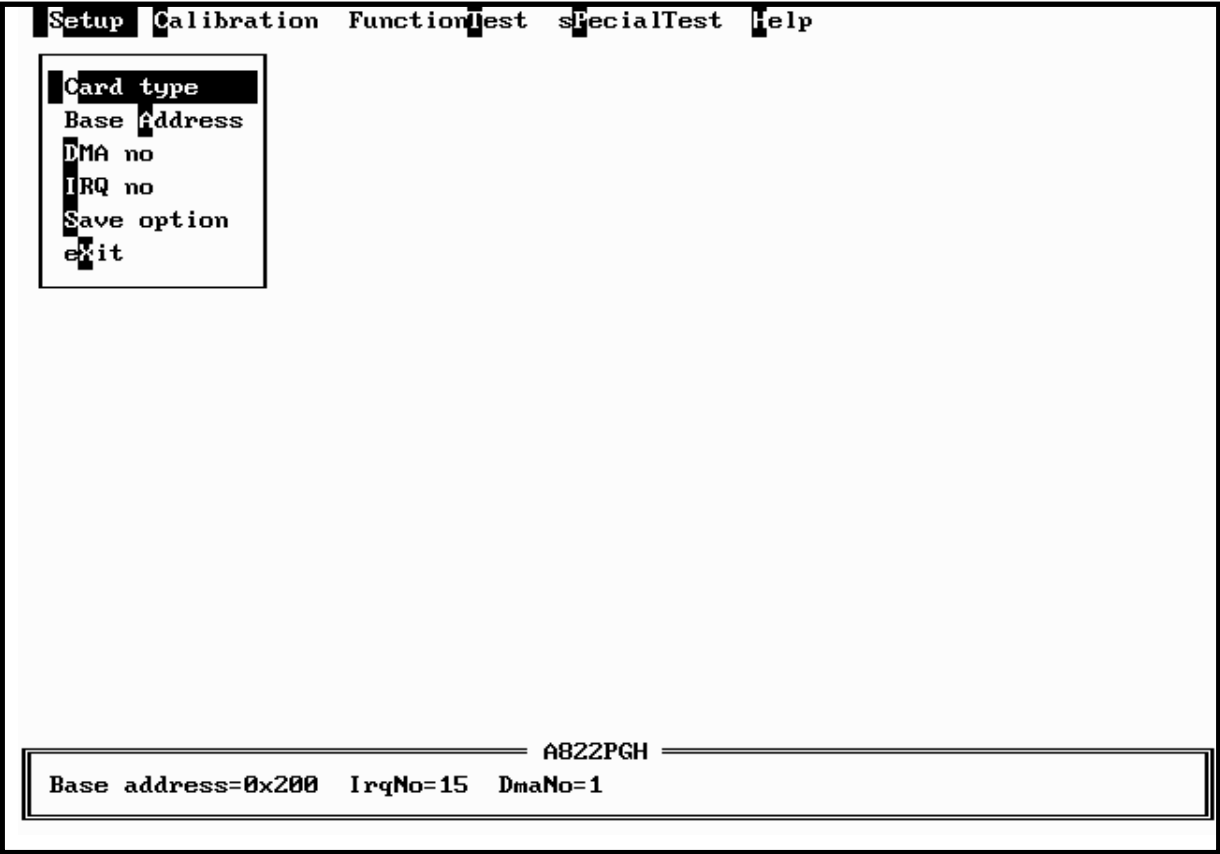


Although you can continue by pressing any key, it is recommended to correct this situation by setting the proper jumper setting. Because many operations occur in the A82XDIAG, the I/O base address is checked first. And if the error occurs, it doesn't work.

---

# 5.2 Running the Diagnostic Utility

The initialization screen of the A82XDIAG is shown as below. As you can see, there are five main menus in the initialization screen. They are Setup, Calibration, Function Test, Special Test and Help. Use the Left or Right key to select the main menu. A main menu that is highlighted means it is selected and some menu items are associated with it. Using the Up or Down key to select the menu items, those menu item will also be highlighted. Alternately, the user can press the command key to highlight the menu item. A command key in a menu item is the character which is highlighted. To proceed with a function associated the highlighted menu item, just press <Enter>. And press <Esc> to abort the current function.



## 5.2.1 Setup

The Setup main menu allows users to setup the board configuration. There are six functions in this item, Card type, Base Address, DMA no, IRQ no, Save option, EXIT.

Card type : <Up/Down> key to select A-826PG, <Enter> key to select

Base Address : <Up/Down> key to select base address, <Enter> key to select

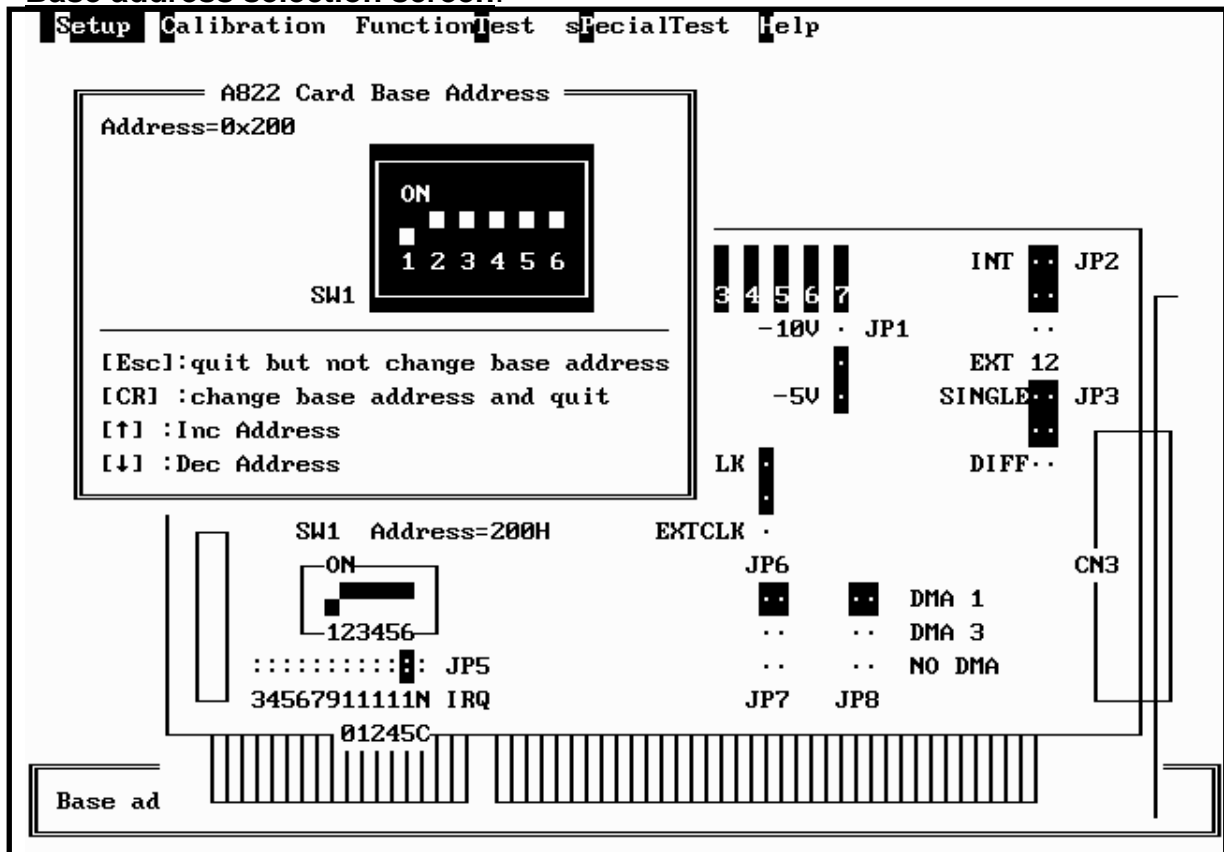
DMA no : <Up/Down> key to select DMA no, <Enter> key to select

IRQ no : <Left/Right> key to select IRQ no, <Enter> key to select

Save option : <Left/Right> key to select yes/no, <Enter> key to select

Exit : <Left/Right> key to select yes/no, <Enter> key to select

### Base address selection screen.



**DMA no and IRQ no selection screen**

Setup Calibration FunctionTest SpecialTest Help

A822 Card DMA No.

DMA=1 JP7 JP8

DMA1 .. ..

DMA3 .. ..

NODMA .. ..

---

[Esc]:quit but not change DMA No.  
 [CR]:change DMA No. and quit  
 [↑][↓]: Change setting

EXTTRG

CN2

SW1 Address=200H

ON

123456

.....: JP5

34567911111N IRQ

01245C

Base ad

1 2 3 4 5 6 7

1 -10V · JP1

2 -5V ·

INT · JP2

EXT 12

SINGLE · JP3

DIFF ·

INTCLK ·

EXTCLK ·

JP6 · · DMA 1

· · · DMA 3

· · · NO DMA

JP7 JP8

CN3

Setup Calibration FunctionTest SpecialTest Help

A822 Card IRQ No.

IRQ=15

.....

.....

3 4 5 6 7 9 1 1 1 1 1 NC

0 1 2 4 5

---

[Esc]:quit but not change IRQ No.  
 [CR]:change IRQ No. and quit  
 [→]:Inc IRQ No.  
 [←]:Dec IRQ No.

SW1 Address=200H

ON

123456

.....: JP5

34567911111N IRQ

01245C

Base ad

1 2 3 4 5 6 7

1 -10V · JP1

2 -5V ·

INT · JP2

EXT 12

SINGLE · JP3

DIFF ·

INTCLK ·

EXTCLK ·

JP6 · · DMA 1

· · · DMA 3

· · · NO DMA

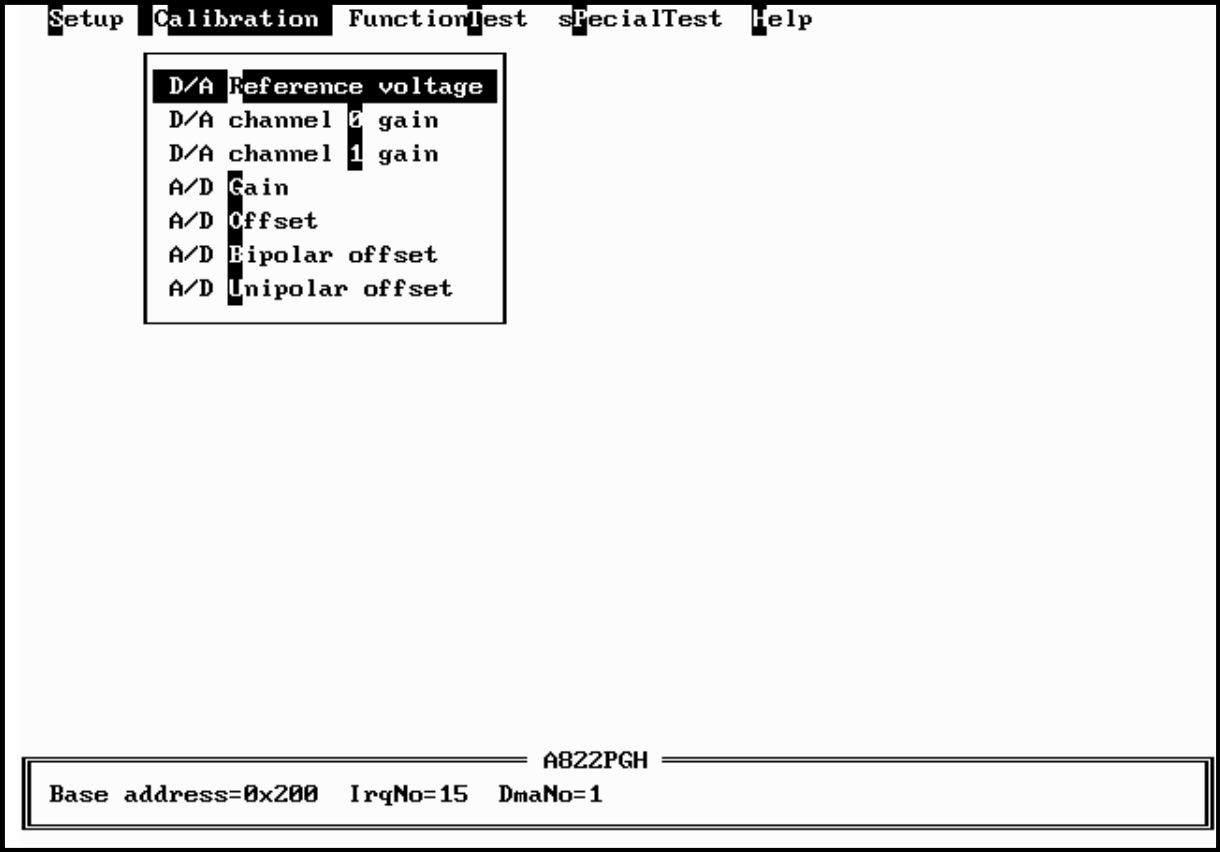
JP7 JP8

CN3

---

## 5.2.2 CALIBRATION

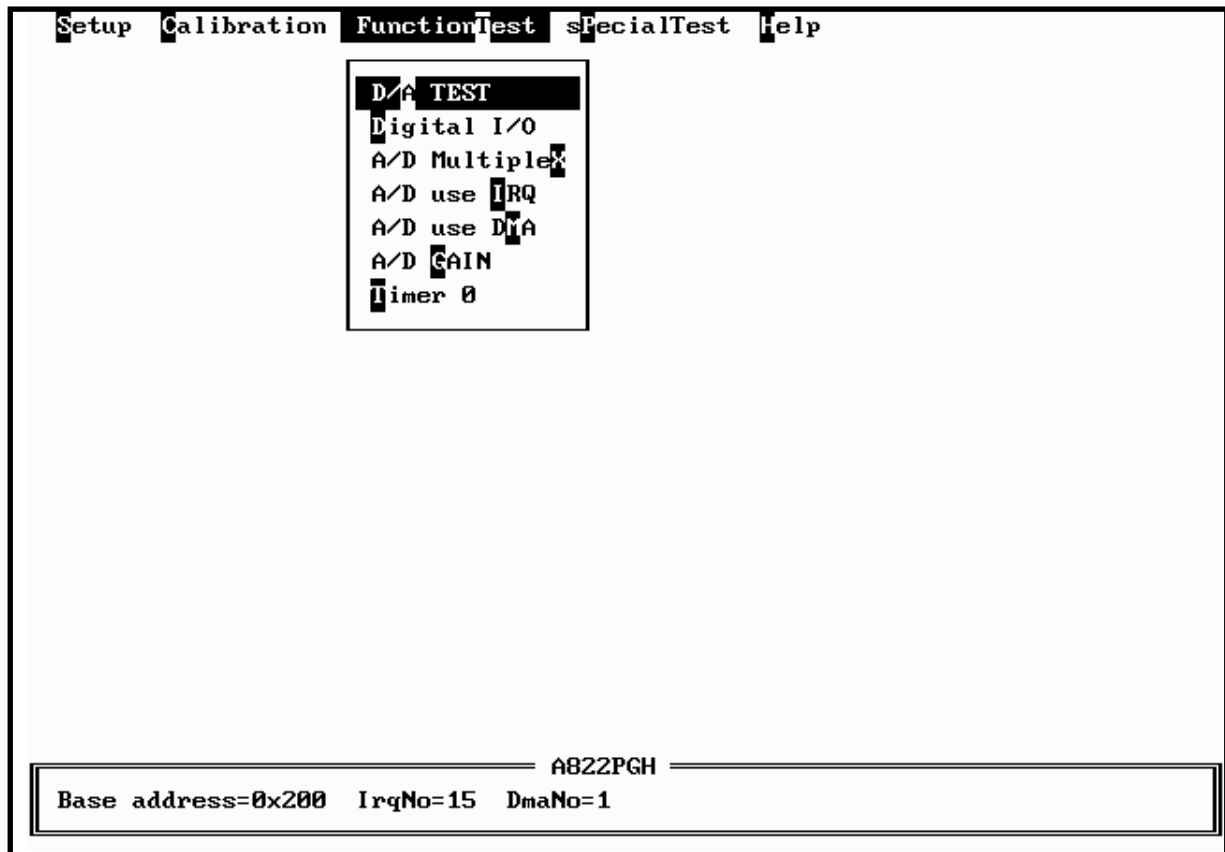
The CALIBRATION main menu contains ten menu items: those are, D/A Reference voltage, D/A Channel 0 gain, D/A channel 1 gain, A/D Gain, A/D Offset, A/D Bipolar Offset, These items are concerning the calibration of the A-826PG. In CALIBRATION main menu, a graphic presentation of the A-826PG board's layout is shown. The calibration will become a visual process in order to reduce user's effort. To keep the optimal performance and correct precision for the board, it is useful to calibrate the board after working for a long time period. There are seven VRs that need to be tuned in calibration process. When you highlight one of the first seven menu items, the associated VR begins blinking. And a message window will appear to direct the user how to tune the VRs. The main menu screen is shown as below.



---

## 5.2.3 FUNCTION TEST

The FUNCTION TEST main menu contains seven menu items: those are D/A TEST, Digital I/O, A/D MULTIPLEX, A/D use IRQ, A/D use DMA, A/D GAIN, Timer 0. The main menu is shown as below.



If selecting “D/A TEST” item, the screen is shown as below.

---

**<D/A TEST > test screen**

```
Setup Calibration FunctionTest SpecialTest Help

          DA Test
-----
Test count=2
  DA channel 1      DA channel 2
-----
  0333H -->  1.000V  0333H -->  1.000V
-----
[p]:pause  [Esc]:quit
[↑]:Inc delay  [↓]:Dec delay  delay= 400

----- A822PGH -----
Base address=0x200  IrqNo=15  DmaNo=1
```

- \* assume D/A output range 0 ~ 5 V
- \* send D/A output to both channels simultaneously
- \* press <p> pause screen, press <p> again release screen
- \* press <Up> key to increase screen delay
- \* press <Down > key to delay screen delay
- \* press <ESC> key to quit

## <Digital I/O> test screen

```
Setup Calibration FunctionTest SpecialTest Help

Digital I/O TEST
Test count=154993
DO      DI      Test count=154993
Hex     Binary  Hex     Binary  Status
-----
[5D70] 0101110101110000 [5D70] 0101110101110000 OK.
[5D69] 0101110101101001 [5D69] 0101110101101001 OK.
[5D6A] 0101110101101010 [5D6A] 0101110101101010 OK.
[5D6B] 0101110101101011 [5D6B] 0101110101101011 OK.
[5D6C] 0101110101101100 [5D6C] 0101110101101100 OK.
[5D6D] 0101110101101101 [5D6D] 0101110101101101 OK.
[5D6E] 0101110101101110 [5D6E] 0101110101101110 OK.
[5D6F] 0101110101101111 [5D6F] 0101110101101111 OK.

Please use 20 pin flat cable connect CN1<->CN2 D= 0
[p]:pause [Esc]:quit [↑]:Inc delay [↓]:Dec delay

A822PGH
Base address=0x200 IrqNo=15 DmaNo=1
```

- \* assume CN1 is directly connected to CN2
- \* a 16-bit up counter is send to 16 channel DO
- \* 16-channel DO directly connected to 16-channel DI
- \* 16-channel DI is readback and show in screen
- \* DO == DI → show OK in screen
- \* DO != DI → show Error in screen
- \* press <p> pause screen, press <p> again release screen
- \* press <Up> key to increase screen delay
- \* press <Down > key to reduce screen delay
- \* press <ESC> key to quit



---

**<A/D Multiplexer> test screen**

| Setup                                     | Calibration | FunctionTest | SpecialTest | Help |
|---|-------------|--------------|-------------|------|
| AD TEST [Polling]                         |             |              |             |      |
| Test count=1515                           |             |              |             |      |
| Channel    Value                          |             |              |             |      |
| -----                                     |             |              |             |      |
| 0        4.795V                           |             |              |             |      |
| 1        3.972V                           |             |              |             |      |
| 2        3.967V                           |             |              |             |      |
| 3        3.301V                           |             |              |             |      |
| 4        4.009V                           |             |              |             |      |
| 5        3.262V                           |             |              |             |      |
| 6        2.651V                           |             |              |             |      |
| 7        1.948V                           |             |              |             |      |
| 8        1.274V                           |             |              |             |      |
| 9        0.925V                           |             |              |             |      |
| 10       0.674V                           |             |              |             |      |
| 11       0.439V                           |             |              |             |      |
| 12       0.356V                           |             |              |             |      |
| 13       0.049V                           |             |              |             |      |
| 14       -0.195V                          |             |              |             |      |
| 15       -0.459V                          |             |              |             |      |
| -----                                     |             |              |             |      |
| A822PGH                                   |             |              |             |      |
| Base address=0x200    IrqNo=15    DmaNo=1 |             |              |             |      |

- \* assume 16-channel single-ended, bipolar, gain=1, analog input signals
- \* input range from -10 V ~ +10 V
- \* continue scanning between 16 channels
- \* press <ESC> key to quit

## <A/D use IRQ> test screen

```
Setup Calibration FunctionTest SpecialTest Help
----- AD TEST [Interrupt] -----
Test count=2
Channel= 0                               C1=10 C2=14 [ 14.3K Hz]
Read AD number= 999/1000                 Max= 4.958 Min= 4.934 Average= 4.942
-----
[000]: 4.939 [020]: 4.939 [040]: 4.949 [060]: 4.946 [080]: 4.941
[100]: 4.937 [120]: 4.939 [140]: 4.949 [160]: 4.951 [180]: 4.941
[200]: 4.944 [220]: 4.939 [240]: 4.939 [260]: 4.944 [280]: 4.944
[300]: 4.941 [320]: 4.941 [340]: 4.941 [360]: 4.941 [380]: 4.951
[400]: 4.944 [420]: 4.939 [440]: 4.939 [460]: 4.944 [480]: 4.941
[500]: 4.941 [520]: 4.939 [540]: 4.939 [560]: 4.944 [580]: 4.941
[600]: 4.941 [620]: 4.941 [640]: 4.941 [660]: 4.941 [680]: 4.946
[700]: 4.946 [720]: 4.941 [740]: 4.941 [760]: 4.941 [780]: 4.939
[800]: 4.939 [820]: 4.937 [840]: 4.939 [860]: 4.941 [880]: 4.941
[900]: 4.941 [920]: 4.939 [940]: 4.941 [960]: 4.941 [980]: 4.951
-----
[p]:pause [Esc]:quit
[PageUp]:Inc channel [PageDn]:Dec channel
[↑]:Inc C1 [↓]:Dec C1 [←]:Inc C2 [→]:Dec C2
-----
A822PGH
-----
Base address=0x200 IrqNo=15 DmaNo=1
```

- \* assume single-ended, bipolar, gain=1
- \* use <PgUp> key to select the next channel
- \* use <PgDn> key to select the previous channel
- \* use <Up>/<Down> key to adjust C1
- \* use <Left>/<Right> key to adjust C2
- \* sampling rate = pacer timer rate =  $2000/(C1 \cdot C2)$  K
- \* use <p> key to pause screen, use next <p> key to release screen
- \* use <ESC> to quit
- \* A/D mode control register=0x06 → select pacer trigger and use interrupt transfer
- \* one cycle sample 1000 A/D data continue
- \* minimal/maximal/average value shown in screen

## <A/D use DMA> test screen

```
Setup Calibration FunctionTest SpecialTest Help
----- AD TEST [Interrupt] -----
Test count=2
Channel= 0                      C1=10 C2=14 [ 14.3K Hz]
Read AD number= 999/1000       Max= 4.958 Min= 4.934 Average= 4.942
-----
[000]: 4.939 [020]: 4.939 [040]: 4.949 [060]: 4.946 [080]: 4.941
[100]: 4.937 [120]: 4.939 [140]: 4.949 [160]: 4.951 [180]: 4.941
[200]: 4.944 [220]: 4.939 [240]: 4.939 [260]: 4.944 [280]: 4.944
[300]: 4.941 [320]: 4.941 [340]: 4.941 [360]: 4.941 [380]: 4.951
[400]: 4.944 [420]: 4.939 [440]: 4.939 [460]: 4.944 [480]: 4.941
[500]: 4.941 [520]: 4.939 [540]: 4.939 [560]: 4.944 [580]: 4.941
[600]: 4.941 [620]: 4.941 [640]: 4.941 [660]: 4.941 [680]: 4.946
[700]: 4.946 [720]: 4.941 [740]: 4.941 [760]: 4.941 [780]: 4.939
[800]: 4.939 [820]: 4.937 [840]: 4.939 [860]: 4.941 [880]: 4.941
[900]: 4.941 [920]: 4.939 [940]: 4.941 [960]: 4.941 [980]: 4.951
-----
[p]:pause [Esc]:quit
[PageUp]:Inc channel [PageDn]:Dec channel
[↑]:Inc C1 [↓]:Dec C1 [←]:Inc C2 [→]:Dec C2
-----
A822PGH
-----
Base address=0x200 IrqNo=15 DmaNo=1
```

- \* assume single-ended, bipolar, gain=1
- \* use <PgUp> key to select the next channel
- \* use <PgDn> key to select the previous channel
- \* use <Up>/<Down> key to adjust C1
- \* use <Left>/<Right> key to adjust C2
- \* sampling rate = pacer timer rate =  $2000/(C1 \cdot C2)$  K
- \* use <p> key to pause screen, use next <p> key to release screen
- \* use <ESC> to quit
- \* A/D mode control register=0x02 → select pacer trigger and use DMA transfer
- \* one cycle sample 1000 A/D data continue
- \* minimal/maximal/average value shown in screen

---

## <DA GAIN> test screen

```
Setup Calibration FunctionTest SpecialTest Help

----- A/D Gain Test -----
GainMode=A822_BI_1                      Count=684
-----
A/D ch0=0x0BFF( 2.498)                  D/A ch0=0x0800( 2.500)
-----
Please connect CN3 pin 1 to CN3 pin 30
              (A/D 0)              (D/A 0)
[Esc]:quit  [↑][↓]:Change Gain
             [←][→]:Change D/A value

----- A822PGH -----
Base address=0x200  IrqNo=15  DmaNo=1
```

- \* assume single-ended, bipolar, gain=1, A/D channel 0 connect to D/A channel 0
- \* use <Up>/<Down> key to adjust gain control code
- \* use <Left>/<Right> key to adjust D/A output value
- \* use software trigger and polling transfer mode
- \* press <ESC> key to quit

---

## <Timer 0> test screen

```
Setup Calibration FunctionTest SpecialTest Help

Timer 0 Test
Timer Mode=3
Value=6C1C
If value is not constant --> Timer is OK.
(CN3 pin 16 : high->low->high->low->... )
[Esc]:quit

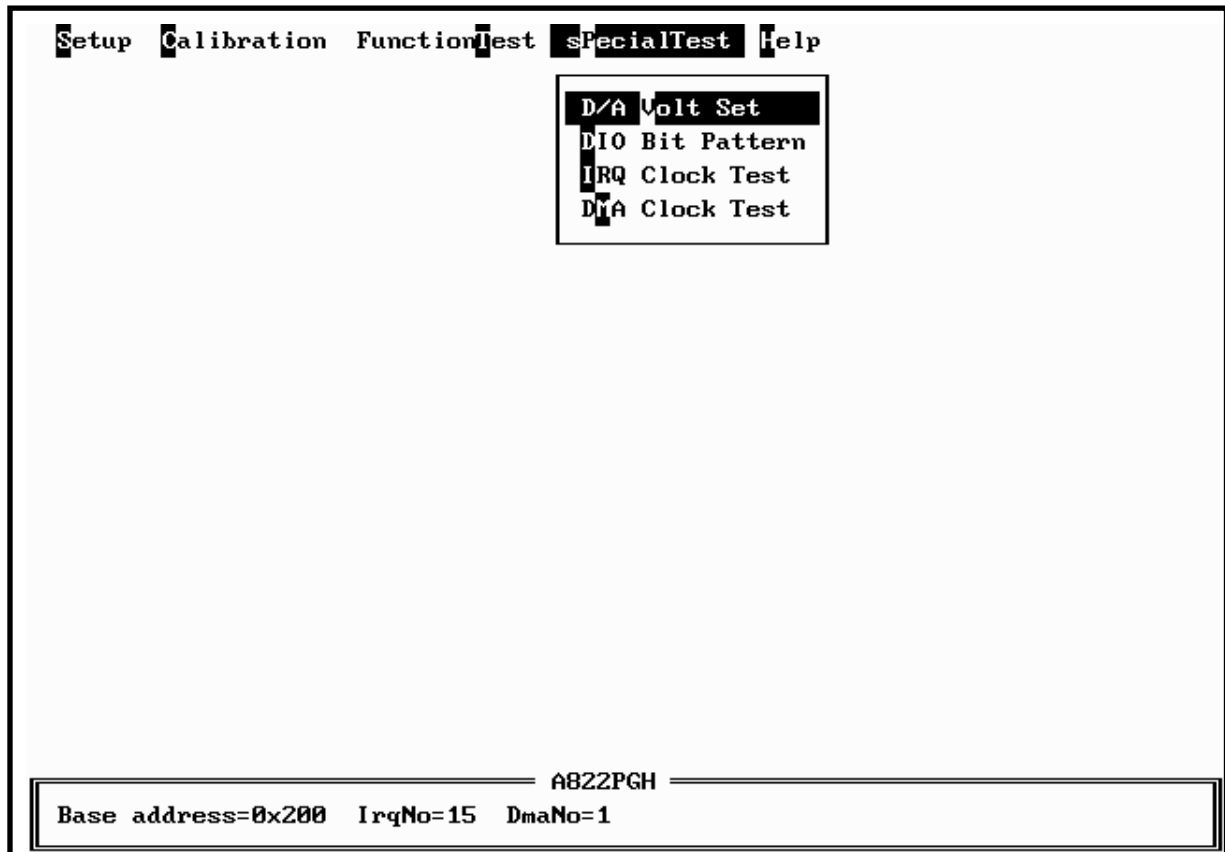
A822PGH
Base address=0x200 IrqNo=15 DmaNo=1
```

- \* assume JP6 select internal 2 M clock
- \* If the counter0 is normal, the value will increment automatically. If the value is a fixed value, the counter0

---

## 5.2.4 SPECIAL TEST

The SPECIAL TEST main menu contains four menu items: those are D/A Volt Set, DIO Bit Pattern, IRQ Clock Test and DMA Clock Test. These functions are reserved for factory testing.



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## 5.2.5 Help

The Help menu will show the software version as below.

